Ageing Simulation of Analogue Circuits and Systems using Adaptive Transient Evaluation

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Abstract—Simulating ageing effects in analogue circuits requires both ageing models and a circuit simulator which is capable of a stress dependent, ageing and recovery aware model evaluation during long term transient simulation. Common approaches on reliability simulation often involve aged models, age precomputation, or lookup tables instead of integrated ageing simulation using memory aware ageing models. Long term transient ageing simulation enhances reliability simulation. This paper presents a framework to model and simulate ageing effects using an adaptive two-times evaluation scheme. This integrates full ageing effect models into behavioural device models. In addition, we introduce semantics for modelling stress levels and ageing parameters in hardware description languages. Our approach is a fully integrated simulation solution, enabling correct and efficient simulation of ageing systems over their lifetimes. We demonstrate how transistor level ageing effects critically affect the operation of a circuit. Our examples incorporate ageing monitors, redundant parts, and self-repair functionality into analogue systems.

I. INTRODUCTION

With increasing integration, ageing effects in electronics introduce lifetime issues. Ageing causes a continuous change of behavioural properties [1]. Often, exposure to stress is responsible and a different stress impact causes differently altered components. Hot carrier injection (HCI) [2] and (negative) bias temperature instability (N)BTI [3] are MOSFET ageing mechanisms. These are subject to the voltages applied to the transistors, and hence depend on the transient operation the whole circuit performs. This is most relevant in analogue circuits, where voltage levels may vary widely due to ageing, and performances are sensitive to parameters.

Current research on reliability evaluation imposes the concept of ‘mission profiling’ [4] to systems. A mission profile specifies the (expected) influences on a system in terms of input signals or levels and environmental conditions on a lifetime scale. Evaluating a system during such a mission involves modelling and simulation challenges. Parameter optimization strategies targeting performances or yield depend on numerical nominal simulation results. Accuracy and speed are critical for the search algorithms.

Physics based simulations reveal the impact on transistor circuits [5], [6]. Recent results [7] show how precomputed fast components of NBTA affect analogue SPICE simulations. For long term considerations, such as implied by mission profiles, neither precomputation nor curve fitting techniques are valid, hence ageing models and circuit simulation need to be reasonably coupled. Nominal ageing simulation can be done by simulating short transients at different times $t_i$, evaluating the ageing models and tracking the impact on the circuits behaviour. Separate ageing model evaluation and ad-hoc simulation loops involving SPICE are common practice e.g. in [8]. Embedded stress level and event-aware step control or efficiency has not been considered yet. Circuit level and system simulation requires faster and higher level ageing models. Available hardware description languages do not provide semantics for ageing effects. Existing workarounds include extra voltage sources [9], or time scaling [10]. Available low level model interfaces in commercial reliability simulators lack expressiveness. Basically, existing approaches do not allow for either accurate modelling or lack efficient long term simulation.

Our contribution is an ageing simulation technique that

- provides nominal analogue circuit and analogue ageing effect evaluation,
- computes long term transients efficiently,
- incorporates an ageing state and stress level and event aware step control,
- enables ageing effects in behavioural models and
- has been implemented as proof of concept based on free software.

II. AGEING EFFECTS

An ageing parameter $p$ describes a property of a circuit subject to change depending on how the circuit is exposed to stress during its lifetime. We define an ageing state as a variable value which is subject to change according to a stress level. Without loss of generality, we let a lower state correspond to a fresher condition. Similarly, a stress level is a variable which depends on the current transient state. A negative rate corresponds to recovery.

The ageing parameter, such as an interface trap state or a behavioural parameter (e.g. an offset shift), is associated to a state vector $z = [z_1, \ldots, z_n]^T$. Each state is controlled by a stress level, a time dependent function $L: [0,t] \rightarrow \mathbb{R}$. We write $L_T$ for the stress level profile restricted to the time interval $[0,T]$ and $z(t) = z(L_T)$ for the value of the state $z$ after the influence of $L_T$. Finally, an ageing parameter is a function $p(z)$ of the state vector.

A. Controlling Decay Processes

Two rate controlled decay processes acting on a set of states in opposed directions form a stochastic process (Fig. 1). This reversely coupled decay (RCD) process is suited to model
time continuous, analogue stress level controlled and recovery aware ageing parameters such as BTI [11]. Its expected value is the defect state \( z \). The equilibrium at stress level 0 is the initial (fresh) value. Exponential functions work well to express the dependency between stress level and transition rate, as they are smooth, always positive and strictly monotonic. If \( L \) is a stress level, the half live times \( \tau_0 \) and \( \tau_1 \) in seconds may be chosen as \( \exp(a \cdot L + b) \) with positive (resp. negative) \( a \) for the transition \( 0 \to 1 \) (and \( 1 \to 0 \) respectively) and suitable \( b \).

III. SIMULATING AGEING EFFECTS

Roughly, an FET is a controlled current source with value \( I_{DS} = K \cdot (V_{GS} - V_{TH})^2 \), where \( K \) is a constant. Some ageing effects cause a gradual shift in threshold voltage \( V_{TH} \). With the notions from Section II, the threshold voltage is a function of the state \( z(t) \) which is determined by the level of stress until \( t \). For simplicity, let \( z \) be just \( [z] \in \mathbb{R}^1 \) and only depend on \( L = [L] = V_{GS}/V \), then \( V_{TH}(t) = V_{TH,0} + \Delta V_{TH} = \exp(z(L(t))) \) for multiple components, we get equations \( f_m \) describing the circuit with the state \( x \) for the node voltages with a dependency on the ageing states \( z \). Ageing states move slower than node voltages, hence the differential equation may be written as

\[
\begin{align*}
  x(0) &= x_0 \\
  f_m(x(t), \partial x(t)/\partial t, \ldots, t, z(t)) &= 0 \\
  z(0) &= 0 \\
  f_z(L(x(t)), z(t), \partial z(t)/\partial t) &= 0.
\end{align*}
\]

The function \( f_z \) holds the equations for the ageing states.

In the above example, \( V_{TH} \) is shifted by an RCD controlled by \( L = V_{GS}/V \), the differential equation for \( z \) turns out to be \( f_z = \partial z/\partial t + c_1 (V_{GS}/V) \cdot z + c_0 (V_{GS}/V) \) [11]. In Fig. 1 we have \( c_1 = \frac{\tau_0}{\tau_0 + \tau_1} \) and \( c_0 = \tau_1 \).

We require that for an ageing effect model, a notion of average stress \( \overline{L} \) exists. Average stress describes the stress impact during short intervals and is locally stable. This exists for integrating models such as \( p(x_T) = \exp\left(\int_0^T L(x(t))\,dt\right) \). RCD processes support an average with similar properties, the equivalent constant stress \( \overline{L} \). The interrelation between \( L \) and \( z \) permits the application of predictor-corrector methods and provides step control measures.

A. A Two-Times Simulator

We compute transients of systems of type of Eq. 1. We factor absolute time into \( t + T \), where \( t \) represents the transient, first-time and \( T \) is the age or second-time. Transient simulations, frames, are executed at increasing second-times \( T_i \), these may vary in length.

![Fig. 1. Example RCD. A stress signal (dotted) and its effect on the expected value of the process. Here, \( \tau_0 = \exp(1-L)s \) and \( \tau_1 = \exp(L)s \).](image)

The times are controlled by the respective next routines. The second-time \( T \) is fixed to the begin of the frame that is currently simulated. The ageing components collect stress levels at each transient step the simulator accepts. The last accept within a frame computes \( L \). The algorithm that controls the second-time is close to a transient simulation loop (Fig. 2). This involves a review procedure, where the components determine their individual maximum tolerable second-time step or schedule events. The discrepancy between the extrapolated average \( \overline{L}_e \) to \( \overline{L}_u \), the average computed from the extrapolated ageing state, is relevant. In the second order case, \( \overline{L}_e \) is obtained using quadratic extrapolation, the review demands \( T_r \leq \text{tol} / (\overline{L}_e(T) - \overline{L}_u(T))^{1/2} \) for the entries \( L \) of \( L \).

B. Behavioural Modelling

The inner workings of an ageing parameter model is beyond the expressive power of widespread hardware description languages. We add the semantics of ageing effects into behavioural modelling languages by means of subdevices and a specially crafted node type (see Fig. 3). Then, using a stress integrator (tt_int), we model ageing effects such as HCI. Other effects, particularly those involving recovery, can be expressed with decay process subdevices. The computation of stress levels from transient states or parameter shifts from states \( z \) does not require language extensions. To represent

![Fig. 2. Adaptive ageing simulation algorithm, naming adopted from Gnucap transient simulation. Dotted bypass: conventional simulation, effectively.](image)

![Fig. 3. Verilog-A implementation of an FET affected by BTI and HCI, simplified for readability. The subdevices used for integration (tt_int) and decay process evaluation (rcd_exp) are not specific to defect mechanisms.](image)
stress Level and ageing State, we stretch the notion of conservative signal flow, defining natures with the corresponding accesses. Model compiler and simulator are aware of the so defined discipline.

IV. APPLICATIONS

We use BSIM 3.3 transistors augmented with HCI and BTI effect models as shown in Fig. 3. The BTI model consists of eight RCD processes spanning eleven decades of effective half live time. For efficiency, we have also incorporated functionally equivalent ageing parameters and subdevices into the C++ code of an existing BSIM 3.3 implementation. Our implementation is based on AdmsXML [13] and GnuCap [14].

A. Circuit Examples

Consider the Halting Problem circuit (Fig. 4, left). The switches $S_g$ and $S_b$ are voltage controlled, and are on at high voltage and have the same threshold. Pushing button $B_1$ enables $P_1$. $P_1$ and $R_1$ are chosen, such that ageing causes the voltage at $nctrl$ drift below the switching threshold, shutting down the circuit. The time of shutdown depends on the degradation state of $P_1$. Its ageing state depends on the stress history. We activate $B_1$ once, at time 0 and simulate until $P_1$ switches itself off. The halting time still depends on the supply voltage. A higher supply voltage causes the transistor to age faster, but then also more damage is required to reach the threshold of $S_l$ and $S_g$.

Monitor circuits can be used to detect circuit failures [15]. Long-term ageing simulation enables the development of analogue on-line monitors. The circuit in Fig. 5 implements an offset monitor connected to a power stage built from source followers. The power stage is symmetric, except for the p- and n-FETs interchanged. These are subject to HCI and NBTI stress. As the nFET's age, the offset voltage lowers, and higher damage on the p-FET side causes a higher offset. A lower levelled signal has more effect on the nFETs, especially on $N_2$. At the beginning, the output offset is rising due to NBTI in $P_1$ and $P_2$. later, HCI catches up. Two monitors track the offset deviation comparing output with the input voltage. Inside the monitor, a trigger is connected to a control node that holds a low-passed peak-difference. Two monitors with interchanged input polarity report too high and too low peak-level offset. In Fig. 6 the circuit is simulated with a sine input signal to the power stage. Power down phases, such as prescribed by a mission profile, interrupt the operation.

Cross coupling two instances of the Halting Circuit we build a redundant circuit (Fig. 7). The instance on the right side uses an nFET. Pulling up the control node (via $p_{ON}$), turns on the unit on the left. The input applied to $p_{IN}$ is an analog signal chosen such that the fresh FET $P_1$ keeps the voltage at $nctrl_1$ above the power-off threshold. This voltage, the low-passed output voltage, will drift down as $P_1$ ages. Consequently, the power supply for the left unit will switch off at some time, pulling down $Dp_1$ through a high pass ($Cp_1$, $R_p1$), activating the complementary unit on the right. During the operation on the right side, $P_1$ is off and recovering from...
TABLE I. **RUN TIMES AND DIRECTED HAUSDORFF DISTANCES TO FINE SAMPLING OF THE EXAMPLE CIRCUITS.**

<table>
<thead>
<tr>
<th>Sampling</th>
<th>Common Source nFET</th>
<th>Halting Circuit</th>
<th>Monitored Amp</th>
<th>Redundancy</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Reference</td>
<td>$\Delta V_{gs}$</td>
<td>$V_{ds}$</td>
<td>$V_{ds}$</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>$10\mu s$</td>
<td>$2\mu s$</td>
<td></td>
</tr>
<tr>
<td>Adaptive</td>
<td>5 ms</td>
<td>0.42%</td>
<td>0.18%</td>
<td>1.7 s</td>
</tr>
<tr>
<td>Equidistant</td>
<td>7 ms</td>
<td>2.95%</td>
<td>1.70%</td>
<td>1.5 s</td>
</tr>
<tr>
<td>Exponential</td>
<td>11 ms</td>
<td>13.96%</td>
<td>7.99%</td>
<td>1.6 s</td>
</tr>
</tbody>
</table>

**V. CONCLUSION**

As the influence of ageing effects is growing with decreasing structure size, accurate nominal simulation and modelling techniques are inevitable. This involves proper algorithms such as two-times simulation of arbitrary ageing effects as well as integration of suitable effect models into hardware description languages. In this paper, we point to a common denominator of ageing effects, behavioural modelling and circuit simulation. On top of this, we have developed a stress level aware adaptive step control scheme to simulate circuits involving ageing effects. This demonstrates feasibility and opens up new possibilities for future reliability studies.

**REFERENCES**


