MINIMUM CURRENT CONSUMPTION TRANSITION TIME OPTIMIZATION METHODOLOGY FOR LOW POWER CTS

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Abstract— the clock tree network can consume up to 40% of the power budget and is one of the limiting factors for realizing low power designs. This paper presents a novel clock transition time optimization based low power clock tree synthesis, for the non-throughput constraint designs. The proposed methodology quantifies the dependence of short circuit and switching power of the buffers on the input clock transition time, with the newly defined “weighted current strength” parameter. The reduction in the weighted current strength parameter value directly maps into the reduction in the total dynamic power of the clock tree. The proposed methodology determines the transition time constraint values for the clock signals which result in the minimum weighted current strength for the synthesized clock tree network. This technique results in up to 34% reduction in the dynamic power of the clock tree network with the existing clock tree synthesis tools and the clock tree library.

Keywords—weighted current strength, short circuit power, switching power, clock tree network, transition time.

I. INTRODUCTION

The clock distribution network is one of the main power consumers in an IC. The clock nets are very large and span entirely over the chip design, they are highly capacitive and their switching activity is very high. The clock network can easily consume 30%-40% of the power budget [1]. Along with the low power requirement, the clock tree network also has to be variability resilient, e.g. Timing margins have to be well defined against process variations. The transition time variance needs to be well controlled in order to prevent the degradation of set up and hold time violations. The need for multi-objective optimization (variation resilience, power minimization and timing closure) makes the clock tree network design very complex.

The minimization of the signal skew at clock sinks has traditionally been the primary objective of clock tree network design. The other design objectives such as area and power consumption are of secondary importance. The most commonly used techniques for low power industrial SoC clock tree synthesis are clock gating [2], Multibit flip-flop (flip-flop merging) [3] and Clock Concurrent Optimization [4]. Clock gating is very mature technology widely utilized for low power clock tree synthesis. It can be employed at all the abstraction levels - system architecture, block design, logic design, and gates. The other technique of Multibit flip-flops (flip-flop clustering) [3] is based on introducing a new kind of flip-flop cells in the clock tree library. Multibit flip-flops designed by sharing clock buffers for the flip-flops enable more compact flip-flop layout area per bit. This clustering results in the reduced numbers of clock sinks and the sinks capacitance in the clock tree network, thereby lowering the power consumption. The Clock Concurrent Optimization [4] technique is based on the modification of clock tree synthesis (CTS) algorithm. The Clock Concurrent Optimization reduces the timing gap arising from the difference in the ideal clocks assumed at the pre-CTS stage and the propagated clocks emerging after the CTS optimization stage. It is a timing driven approach compared to the traditional skew driven CTS methodologies. This approach simultaneously optimizes both clock and logic delays using a single cost metric.

The integration of the above mentioned techniques in the CTS flow results up to 25% reduction in the clock tree dynamic power with the commercial EDA tools. The commercial EDA are tools driven by the high performance requirements of achieving zero skew and sharper transitions for a given timing closure. This results in the synthesis of an overdesigned clock tree network utilizing higher number and higher drive strength buffers with very high switching power, especially for the non—throughput constraint designs (<100 MHz). A guiding methodology is required for achieving low power clock tree synthesis, especially for non-throughput constraint designs. This guiding methodology should not introduce new cells or CTS algorithm considering tighter timing and costs budget associated with the industrial SoC designs.

The quality of the synthesized clock tree distribution network is highly dependent on the CTS algorithm, leaving little or no freedom for the physical designers. However, the clock tree constraint engineering has significant impact on the clock distribution network. The clock tree constraint engineering consists of the optimization of the clock
constraints such as the transition time, buffers usage, skew etc. The proposed solution is based on the clock tree transition time constraint optimization for synthesis of low power clock tree network.

The clock tree network consists of wires, clock buffers, gating cells and clock sinks (flip-flops). The power consumption of clock tree building blocks consist of switching power and short circuit power (Fig.1). The clock transition time [5-6] optimization plays a crucial role in the determination of the power consumption of the clock tree networks (Fig.1). The sharper transitions for the clock tree synthesis, result in the usage of higher number of buffers and also the utilization of larger sized clock tree buffers is high. This increase the switching power for the clock tree buffers. Alternatively, sloppy transitions for the clock tree synthesis decrease the switching power for the clock tree buffers (utilization of the fewer number of buffers and also the smaller sized buffers are utilized). However, this result in the risk of increased short circuit power for the clock tree buffers [1]. This dependency of the clock transition time on the synthesis of the clock tree network can be exploited for the optimization of the switching and the short circuit power, especially for the non-throughput constraint designs. The optimized transition time constraint results in the low power clock tree network synthesizes.

II. TRANSITION TIME OPTIMIZATION METHODOLOGY

The proposed methodology defines a new parameter, the weighted current strength (WCS) eq (1), which determines the impact of the clock transition time on the total power consumption of the clock tree buffers. The WCS quantifies the impact of the buffers sizes (increased switching power) and sloppy transitions (increased short circuit power) with respect to the most ideal scenario - clock tree network utilizing a smallest drive strength clock tree inverter in a given technology (minimum switching power), driving the zero output load and with an input transition which yields the minimum short circuit power.

\[
WCS = \sum_{i=1}^{n} \frac{I_{BUFdrv}(i)}{I_{MIN}}
\]

\[
I_{BUFdrv}(i) = \frac{I_{BUFdrv}(tr)}{I_{MIN}}
\]

TABLE I. LOOK UP TABLE FOR THE INPUT TRANSITION & NORMALIZED\(^a\) AVERAGE CURRENT\(^b\)

<table>
<thead>
<tr>
<th>Interval Range (ps)</th>
<th>2x</th>
<th>4x</th>
<th>6x</th>
<th>8x</th>
<th>12x</th>
<th>16x</th>
<th>24x</th>
</tr>
</thead>
<tbody>
<tr>
<td>Tr1 (10-100)</td>
<td>3.14</td>
<td>6.28</td>
<td>9.43</td>
<td>12.56</td>
<td>18.84</td>
<td>25.12</td>
<td>37.76</td>
</tr>
<tr>
<td>Tr2 (100-200)</td>
<td>2.96</td>
<td>5.91</td>
<td>8.87</td>
<td>11.82</td>
<td>17.74</td>
<td>23.65</td>
<td>35.54</td>
</tr>
<tr>
<td>Tr3 (200-400)</td>
<td>2.92</td>
<td>5.82</td>
<td>8.72</td>
<td>11.65</td>
<td>17.48</td>
<td>23.3</td>
<td>35.02</td>
</tr>
<tr>
<td>Tr4 (400-600)</td>
<td>2.9</td>
<td>5.8</td>
<td>8.7</td>
<td>11.62</td>
<td>17.43</td>
<td>23.24</td>
<td>34.93</td>
</tr>
<tr>
<td>Tr5 (600-900)</td>
<td>2.92</td>
<td>5.82</td>
<td>8.72</td>
<td>11.65</td>
<td>17.48</td>
<td>23.3</td>
<td>35.02</td>
</tr>
<tr>
<td>Tr6 (900-1150)</td>
<td>2.99</td>
<td>5.96</td>
<td>8.97</td>
<td>11.95</td>
<td>17.92</td>
<td>23.9</td>
<td>35.91</td>
</tr>
</tbody>
</table>

\(^a\)Normalized w.r.t to minimum sized inverter of library operating at minimum current consumption.

\(^b\)Mean of current consumption at lower bound of timing range and higher bound is taken as the value of average current consumption for a given interval range.

The objective is to find a maximum clock transition constraint which results in the minimum WCS valued synthesized clock tree network. This requires the construction of look-up tables for the clock buffers current consumption (40nm LP CMOS) as a function of input transition time (Table 1). This is constructed from the spice simulation of the buffers in the clock tree library for the different input transition values. For every interval range, the mean value of the current consumption at a lower bound and the higher bound of the timing range is computed which is then normalized with respect to the current consumption of a minimum sized clock tree inverter operating at the minimum current consumption. This normalization is done for benchmarking with respect to the idea scenario, a clock tree network with a minimum sized clock tree inverter driving zero load and the input clock transition resulting in the minimum current consumption. The transition intervals Tr3 – Tr5 are the minimum current consumption intervals for the different drive strength clock tree buffers.

After the CTS stage of the place and route (PNR), list of the clock tree buffers with their input transition is extracted.
TABLE II. BUFFER TRANSITION COUNT TABLE.

<table>
<thead>
<tr>
<th>Buffer Drive Strength</th>
<th>Tr1</th>
<th>Tr2</th>
<th>Tr3</th>
<th>Tr4</th>
<th>Tr5</th>
<th>Tr6</th>
<th>Tr7</th>
<th>Tr8</th>
</tr>
</thead>
<tbody>
<tr>
<td>24x</td>
<td>15</td>
<td>2</td>
<td>3</td>
<td>2</td>
<td>2</td>
<td>17</td>
<td>9</td>
<td>4</td>
</tr>
<tr>
<td>16x</td>
<td>16</td>
<td>5</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>4</td>
<td>2</td>
</tr>
<tr>
<td>12x</td>
<td>23</td>
<td>9</td>
<td>24</td>
<td>12</td>
<td>0</td>
<td>3</td>
<td>2</td>
<td></td>
</tr>
<tr>
<td>8x</td>
<td>0</td>
<td>0</td>
<td>7</td>
<td>18</td>
<td>35</td>
<td>0</td>
<td></td>
<td></td>
</tr>
<tr>
<td>6x</td>
<td>2</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>6</td>
<td>3</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>4x</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>4</td>
<td>0</td>
<td></td>
</tr>
<tr>
<td>2x</td>
<td>3</td>
<td>3</td>
<td>5</td>
<td>2</td>
<td>2</td>
<td>11</td>
<td>6</td>
<td>11</td>
</tr>
</tbody>
</table>

A. Generated by extracting clock transition time slopes post CTS stage, reference design of 165K gates in LP CMOS 40Technology.

Then the buffers of different drive strength depending on their input clock transition are sorted into buffer transition count table. The buffer transition count for a given transition time interval (Tr) is the number of times a given buffer receives the input clock with the transition time lying in the transition time interval (Tr). Table II, shows a buffer transition count table generated from the extraction of the input clock transition value of the propagated clock for the different drive strength buffers utilized in the clock tree network after the CTS stage. For example, the buffer transition count value of 9 for the 24x drive strength buffers in the clock tree network for the transition interval range Tr7 (650-900)ps means that there are 9 buffers of drive strength 24x in a clock tree network for which the input clock transition lies in the timing interval Tr7.

The I BUFdrv (tr) , for a given timing interval and drive strength is obtained by a product of the buffer transition count and the normalized average current value for the timing interval Tr and the given drive strength. For example, I BUFdrv (Tr7) for 24x drive strength buffer is the product of the buffer transition count (9), obtained from the generated transition count table with the normalized current consumption value of the timing interval Tr7 (35.91), obtained from Table I. The summation of the products of the buffer transition counts, extracted from the clock tree network for a given drive strength with its normalized average current values, determines the total normalized current consumption contribution I BUFdrv (i) for a given drive strength buffer in the synthesized clock tree network. For example, I BUFdrv (24x) summation of the products of buffer transition count values with the normalized current values for transition interval range Tr1-Tr8 is 1842.09. The weighted current strength is obtained by addition of I BUFdrv (i) values for all the n different drive strength buffers utilized in the clock tree network. The weighted current strength measures the combined impact of buffer switching power and the short circuit power. The reduced weighted current strength value of the clock tree network means that the clock tree network has lower switching and the short circuit current consumption.

The sloppy transitions and reducing the higher drive strength buffer options result in the minimum energy consumption clock tree network. The clock tree synthesis with the full range of clock tree library cells versus partial range eliminating the higher drive strength buffers, impacts the clock tree network topology in a manner that it reduces the total drive strength of clock tree network and shifts the clock transition time towards the minimum current consumption transition time interval ranges. The decimation of clock tree library with only small/medium drive strength buffers ( ≤ 8x/12x drive strength) buffers reduce the total drive strength of clock tree network by ~30% compared to the clock tree network synthesized with the full range of clock tree library cells (2x – 32x drive strength) for the same timing closure (Fig 2a). The commercial EDA tools with the full range of clock tree library cells synthesis clock tree network with the sharper clock transitions for a given value of maximum clock transition constraint parameter. The clock tree library, with only small drive strength buffers (≤ 8x drive strength) for the same given value of maximum clock transition constraint shifts the clock transition slopes towards minimum current consumption transition interval ranges (Fig.2b). The transition intervals Tr3 and Tr4 are preferred over Tr5 as a margin protection against the clock slope degradation caused by the parasitics at the SIGNOFF stage.

The whole idea of transition time constraint value relaxation and clock tree library decimation to small/medium drive is to reduce the total drive strength of clock tree network, and the maximize the clock tree buffers operating in the...
minimum current consumption interval range. The clock transition timing constraint is relaxed to the point that it synthesizes minimum WCS clock tree network topology, with the timing closure.

The hierarchy of the clocks is also taken into account for the maximum clock transition time constraint parameter relaxation. For the source clocks (up in the hierarchy) maximum clock transition time constraint values are relaxed less compared to the generated clocks (lower in the hierarchy). The stricter maximum clock transition time constraints value for the clocks lower in the hierarchy compared to the clocks up in the hierarchy act as a transition time wall which dictates the sharper input clock tree slopes for the all the clocks. This results in a convergence problem (non minimum un optimized weighted current strength value) for the minimum current consumption based clock tree synthesis.

Fig. 3 shows the weighted current strength for the synthesized clock tree network. Relaxed clock transition constraint value of 400ps results in the lower WCS clock tree network compared to MT of 200ps. The choice of clock transition constraint value of 400ps shifts the clock transitions towards minimum current consumption interval range resulting in the synthesis of low power clock tree network. The weighted current strength value decreases from ~15,600 to ~12379 by shifting MaxTran value by 200ps. The clocks high in hierarchy (source clocks) have less relaxed transition time constraint compared to the clocks which are low in hierarchy (generated clocks). This is because of the more clock signal propagation for source clocks compared to generated clocks. The source clock network has to span more levels and is more prone to cross coupling induced timing issues. In addition to that the stricter transition constraints for the generated clocks compared to the source clocks result in an un optimized weighted current strength value because of the transition wall created by the stricter MT values of the generated clocks. By constraining the source clocks stricter compared to the generated clocks results in further reduction of WCS to ~9770 with timing closure.

A. Impact on Clock Tree Network

The relaxation of clock tree transition constraint parameter results in an increased number of clock sinks in the clusters to be driven by a given buffer node. The corresponding fan-out distribution with increased cluster size results in the reduction of number of wire segments. Fig. 4 shows the impact of clock maximum transition parameter on the wiring load of the synthesized clock tree network topology. The clock maximum transition parameter value of 400ps (minimum WCS clock tree network) results in ~18% reduction in the wiring load capacitance compared to the clock tree network synthesized with 100ps clock maximum transition value.

B. Impact on Clock Sinks

The minimum WCS clock tree network is based on the relaxation of the clock transition constraint value which results in the sloppy transitions. The sloppy clock transitions increase the T_{C-Q} (clock to output) delay of the flip-flops used in the clock tree network. The degradation of T_{C-Q} delay with the sloppy input clock transition requires upsizing of the data path combinational logic for the timing closure. But for the target frequency performance of tens of MHz, this is a less of an issue as there is enough positive timing slack available. Fig. 5. shows the impact of input clock transition time on the average current consumption of the flip-flops and the T_{C-Q} delay. The minimum WCS yielding transition constraint time is (5-7.5) % of the clock period (non-throughput constraint designs, < 100 MHz). The corresponding T_{C-Q} delay is (10 -12.5) % of the timing budget and the available positive timing slack for the timing closure is sufficiently large to prevent the upsizing of data combinational
C. Impact on Clock Skew

The maximum skew requirement is satisfied for the allowed optimization range of the maximum clock transition time constraint value (Fig.6). The maximum defined skew limit of 400ps is satisfied for the entire range of synthesized clock tree network for 100ps-600ps of the input transition time constraint and the clock period of 10ns. The minimum WCS based clock tree network synthesis.

III. CONCLUSION

The minimum WCS based clock tree synthesis for an industrial test case, 165 K gates and 20K clock sinks in 40nm LP CMOS technology (Fig.7), results in 34% reduction in the clock tree network power. The minimum WCS is achieved with the maximum clock transition time of 375ps for the source clocks and the 525ps for the generated clocks. The decimated clock tree library utilized for the clock tree synthesis has the highest drive strength limited to 8x buffer/inverter size. The transition constraint value based on WCS minimization in 40nm LP CMOS can be applied to wide range of non-throughput constraint design cases.

The minimum WCS based clock tree synthesis solves a critical problem of low power clock tree network for non-throughput constraint designs with the commercial EDA tools. The minimum WCS based clock tree synthesis is a constraint engineering based design approach. It does not require any modifications in the algorithm or introduction of new clock tree library cells. The analysis based on the realistic test case in 40nm LP CMOS technology and for the maximum operating frequency of 100MHz results in a predictive CTS constraint definition methodology which can be applied to new design cases with the same range of operating frequency and technology, in order to obtain desired low power clock tree network.

REFERENCES