DATE 2015 University Booth

The University Booth is organised during DATE and will be located in booth 4 of the exhibition area. All demonstrations will take place from Tuesday, March 10 to Thursday, March 12, 2015 during DATE. Universities and public research institutes have been invited to submit hardware or software demonstrators.

The University Booth programme is composed of 39 demonstrations from 14 different countries, presenting software and hardware solutions. The programme is organised in 11 sessions of 2 or 2.5 h duration and will cover four major topics:

- Electronic Design Automation Prototypes
- Hardware Design and Test Prototypes
- Designing Electronics for the Internet of Things
- Designing Electronics for Medical Applications

The University Booth at DATE 2015 invites you to booth 4 to find out more about the latest trends in software and hardware from the international research community.

Several demonstrators will be shown more than once, giving visitors more flexibility to come to the booth and find out about the latest innovations.

We are sure that the demonstrators will give an attractive supplement to the DATE conference program and exhibition. We would like to thank all contributors to this programme.

More information can be found online at http://www.date-conference.com/group/exhibition/u-booth. A University Booth programme flyer will be included in the conference bags. The following demonstrators will be presented at the University Booth.

3D-COSTAR: USING 3D-COSTAR FOR 2.5D-/3D-SIC COST ANALYSIS

Mottaqiallah Taouil[1], Mottaqiallah Taouil[1], Said Hamdioui[1] and Erik Jan Marinissen[2]
[1]TU Delft, NL; [2]IMEC, BE

Abstract: *Selecting an appropriate and efficient test flow for a 2.5D/3D Stacked IC (2.5D-SIC/3D-SIC) is crucial for overall cost optimization. In this demonstration, we present 3D-COSTAR, a tool that considers costs involved in the whole 2.5D/3D-SIC chain, including design, manufacturing, test, packaging and logistics, e.g. related to shipping wafers between a foundry and a test house; and provides the estimated overall cost for 2.5D/3D-SICs and its cost breakdown for a given input parameter set, e.g., test flows, die yield and stack yield. Several case studies will be presented in which the overall cost and product quality (in defective parts per million) are analyzed.*

4-LOOP: 4-CORE LEON 3 WITH LINUX OPERATING SYSTEM, OPENMP LIBRARY AND HARDWARE PROFILING SYSTEM

Giacomo Valente, Vittoriano Muttillo and Fabio Federici, University of L'Aquila, IT

Abstract: *Multi-processor SoC based on soft-cores are increasing the range of applications that could be implemented by exploiting FPGAs. In this context, this demo presents a symmetric multi-processor system, composed of four Leon 3 cores and a custom Linux kernel, able to execute OpenMP-based applications and enhanced with a hardware profiling system. OpenMP support and the novel profiling system are the results of R&D activities conducted by several students and Professors at University of L'Aquila.*

A FRAMEWORK FOR THE EMULATION AND PROTOTYPING OF NANO-PHOTONIC OPTICAL ACCELERATORS

Alberto Garcia-Ortiz[1], Wolfgang Büter[2], A. Ali[3], S Mahmood[3], S. Arefin[3], V. V. Parsi Sreenivas[3], M. Mike Bülters[4] and R.-B. Bergmann[4]
[1]University of Bremen, DE; [2]Institute for Electrodynamics and Microelectronics Systems (ITEM), DE; [3]University of Bremen, Physics/Electrical Engineering, DE; [4]Bremer Institut für angewandte Strahltechnik GmbH, DE

Abstract: *The recent advances in on-chip optical communication anticipate nano-photonic optical computing as a disruptive new technology. Different architectural solutions and competing physical implementations are currently being investigated. They include a wide spectrum of approaches such as those based on optical analog processing (e.g., nano-photonic optical vector-matrix multiplication), digital optical gates (e.g. reversible nano-photonic gates, BDD-based approaches, etc) or even quantum computing. Since the computing, performance, and error characteristics of these technologies differ substantially from those of standard CMOS technologies, an early co-design framework for nano-photonic accelerators embedded with digital multiprocessor systems is urgently required. It should allow an early*

investigation about the possible implementation of some kernels using optical accelerators and the effect of optical non-idealities in the overall system. This demo presents a framework for the virtual emulation and prototyping of nano-phonic accelerators for optical analog processing and optical digital gates, currently being developed at the "Institute of Electrodynamics and Microelectronics" (ITEM) and at the "Bremen Institute for Applied Beam Technology" (BIAS). This framework, based on the ideas of rapid prototyping and virtual emulation using FPGA technology, provides two levels of operation. At a first level, it offers a library of models that can be used to construct a virtual prototype of a hybrid multi-processor and nano-photonic system. The parameterizable models emulate several optical non-idealities but are synthesizable at the RTL-level, so that a standard FPGA-emulation of the complete system can be carried out. In a second level, it offers the possibility to plug-in a macroscopic optical accelerator to prototype the nano-photonic one with higher accuracy. In order to illustrate these two levels of operation, the demo at the DATE University-Booth will be twofold. Virtual emulation demo In the first demo, the user can define the functionality of the optical accelerator. Using a reversible-toolchain based on the RevKit tools by the "Computer Architecture and Reliable Embedded Systems" (AGRA), a reversible implementation is created. The structural reversible implementation is transformed into a nano-photonic model which is emulated in a FPGA. The final system, composed by a standard processor communicating with the nano-photonic model of the accelerator, can be programmed in C so that the user can study the impact of the accelerator in its algorithm. Physical prototype-demo This demo focuses on the prototype of a low-cost vector-matrix multiplication core using optical processing. The optical prototype is composed by a sandwich of two LCD structures with orthogonal polarizations sending an image to an integrated camera. The different elements are controlled by a hardware IP and connected to an embedded processor. The user can define several parameters of the optical processor, such as the spot-size, the photo-detector pitch etc. The physical prototype is then configured to that mode, and used as an optical accelerator by a microprocessor embedded in a FPGA. Again the user can program some C algorithms to study the system performance. Additionally a link to Matlab® allows the analysis of the precision achieved by the optical vector-matrix-multiplication process.

AIDASOFT: ANALOG IC DESIGN AUTOMATION

Nuno Horta[1], Nuno Lourenço[1], Ricardo Martins[1], Ricardo Póvoa[1], António Canelas[1], Ricardo Lourenço[2] and Pedro Ventura[2]
[1]Instituto de Telecomunicações/Instituto Superior Técnico, PT; [2]Instituto de Telecomunicações, PT

Abstract: *This demo presents AIDA an ongoing project at Instituto de Telecomunicações/University of Lisbon, Portugal, which addresses analog IC design automation from circuit-level specifications to layout descriptions in GDS-II. AIDA consists of two main modules AIDA-C and AIDA-L. AIDA-C is demonstrated for layout-aware circuit-level sizing and optimization by generating a family of robust Pareto Optimal solutions. AIDA-L is demonstrated by generating the layout taking into account electrical currents information to mitigate electromigration and IR-drop effects, and also wiring symmetry for multiport multi-terminal signal nets of analog ICs.*

AN FPGA LAB-ON-CHIP: AN ANALYSIS TOOL AND FRAMEWORK FOR ADVANCED MEASUREMENTS AND RELIABILITY ASSESSMENTS ON MODERN NANOSCALE FPGAS

Petr Pfeifer, Technical University of Liberec, CZ

Abstract: *Wide portfolio of new technologies in design and manufacturing of advanced integrated circuits enables higher integration of complex structures at ultra-high nanoscale densities, but also sensitivity to various changes of the internal nanostructures and their parameters, resulting in the requirement of advanced reliability assessments. The developed and presented revolutionary new set of tools enables complex lab-on-chip solutions in nanoscale FPGAs and it allows easy implementation of tasks like completely on-chip internal parameter measurements in FPGAs, actual structure delays with respect to environmental parameters, device and platform identification, validation of selected design parameters, identification of crosstalk path and mutual impacts, as well as various changes in internal parameters. It actively supports design reconfiguration. The set of tools can be used for fast standalone or system built-in post-production device and platform parameter and quality checking and validation, parameter-aware placement and routing of critical design parts and performance optimization of existing designs, device aging identification and measurement, active and online data generation for reliability assessments and design reliability enhancements. It is available for FPGAs from 90nm down and will be demonstrated on advanced 28nm Xilinx FPGAs.*

BONDCALC: THE BOND CALCULATOR

Carl Christoph Jung[1], Christian Silber[2] and Juergen Scheible[1]
[1]Reutlingen University, DE; [2]Robert Bosch GmbH, DE

Abstract: *The Bond Calculator is a fast and exact tool to help designers to choose a bond wire, which does not fuse. The Bond Calculator is orders of magnitude faster than FEM and Easy-to-use. The Bond Calculator helps designers to estimate the temperature at the bond connection itself, by calculating the time and space dependence of the power delivered from the bond wire to the chip. These temperature changes can affect the durability of the bond connection. The Bond Calculator uses a simplified simulation model to calculate the temperature profile in a bond wire from the induced current profile. This software tool has been validated by FEM and measurement.*

COMBINATION OF WSN AND 1ST ORDER KINETIC MODEL FOR REAL-TIME SHELF-LIFE PREDICTION OF PERISHABLE GOODS

Valerio Francesco Annese and Daniela De Venuto, Politecnico di Bari, IT

Abstract: *A complete and autonomous multi-sensing platform for perishable goods monitoring and shelf-life prediction, based on the combination of the wireless sensor network (WSN) technology and a further real-time data processing, is presented. The proposed approach offers an effective solution for waste and losses reduction in the supply chain of perishable products and, thus, an improvement of food safety, as well as food organoleptic qualities: in fact, we demonstrate the possibility to predict products shelf-life from the environment parameters such as temperature, relative humidity and light exposition in real-time. Although several models for shelf-life prediction have been already developed, none of them was embedded in a complete system supported by the real-time data availability, offered by an "ad hoc" WSN. In our infrastructure, system integration issues are carefully solved: data collected by the WSN are firstly uploaded on a cloud. An appropriate Java application makes these data available to any kind of elaboration. Then, we developed an algorithm that implements a 1st order kinetic model of the quality decay reaction, employed to evaluate remaining shelf-life of the monitored perishable product. The model takes into account the dependence of the degradation rate from the temperature according to Arrhenius law. To validate the platform we have conducted several case studies. Here we propose an 8-days monitoring of a warehouse of vegetable products (fresh tomatoes): the real-time shelf-life prediction was calculate through data coming from six multi-sensing nodes that were monitoring several environmental conditions in which the products were subjected. The implementation of the algorithm in an application for any kind of portable and non-portable devices (just like an iPad, smartphones, etc.) would result in a widespread diffusion of this technology. It is worth to notice that the complete infrastructure is a suitable low-cost and easy to implement solution for monitoring any perishable product (such as beverages, drugs, vaccines, blood, etc.) stored in any environmental condition (warehouse, transportation, store, etc.).*

CRYPTOCHIP: DEMONSTRATION OF CRYPTOGRAPHIC ASIC PROTOTYPE

Xuan Thuy Ngo, Xuan Thuy Ngo, Jean-Luc Danger, Sylvain Guilley, Tarik Graba, Yves Mathieu and Zakaria Najm, Télécom ParisTech, FR

Abstract: *We want to demonstrate a cryptographic ASIC implemented in ST 65nm technology. It features the following IPs: - Open Loop True Random Number Generator (TRNG). - Loop Physical Unclonable Function (PUF). - SRAM PUF. - Secure Clock. - Digital Sensor. - Advanced Encryption Standard (AES) with Piret-Trojan. - Active Shield. The demo consists in presenting the functionality and the security level of some of those IPs.*

DESIGNING AND EVALUATING RESOURCE MANAGEMENT POLICIES FOR HETEROGENEOUS SYSTEM ARCHITECTURES

Gianluca Durelli, Cristiana Bolchini, Antonio Miele, Gabriele Pallotta, Marcello Pogliani and Marco Santambrogio, Politecnico di Milano, IT

Abstract: *Current trends in computing architectures are going in the direction of heterogeneous systems (i.e. constituted by CPUs, GPUs, and FPGAs). The design space to effectively exploit these platforms is huge. Within this context, research is moving towards systems able to adapt themselves to a wide range of workloads to optimize performance/energy trade-offs. We propose a virtual platform (VP) to help designers to develop adaptive policies. The VP allows to perform an high-level evaluation of the policies with the possibility to customize both the architecture and the workload mix.*

FLARE: A RECONFIGURATION AWARE FLOORPLANNER

Riccardo Cattaneo, Marco Rabozzi and Marco Santambrogio, Politecnico di Milano, IT

Abstract: *This demonstration presents a floorplanner tool addressing partially-reconfigurable FPGAs. The input of the tool consists of a set of regions described in terms of their heterogeneous resource requirements together with the number of interconnections among regions and the target FPGA of the partial reconfiguration (PR) design. Once the input are specified, the floorplanner allow the designer to manually or automatically perform the floorplan of the regions.*

FUNCTIONAL ECO: AN EFFICIENT REWIRING ENHANCED FUNCTIONAL ECO

Tak Kei Lam[1], Xing Wei[2], Yi Diao[2], Tak Kei Lam[1] and Yu-Liang Wu[2]
[1]The Chinese University of Hong Kong, HK; [2]Easy-Logic Technology Limited, HK

Abstract: *Circuit designs have been much more complex nowadays. Bugs and/or specification changes often happen in late design cycles. Running the whole design cycle again is time consuming and costly. Functional engineering change order (ECO), which is the process that patches an old implementation to accomplish a new specification, is therefore performed instead to save time and cost. In an ECO effort, minimizing the patch size is crucial since it gives a higher chance of successful insertion and minimal perturbation to a near or completely committed EDA outcome (e.g. satisfaction on area and timing constraints). However, an ECO work can be very difficult at this stage as the combinational signals of the old specification may have vanished after iterations of synthesis and optimizations. We*

implemented a practical prototype for functional ECO. Our result outperforms all results publicized in the ICCAD 2012 Contest.

GESTURE RECOGNITION BASED ROBOTIC EMBEDDED SYSTEM

Seetal Potluri[1], Ravindran Balaraman[1], Pradyot K. V. N.[1], Manimaran S. S. [1], Praharasan Raja[1], Anshul Bansal[2] and Abhishek Mehta[2]
[1]IIT Madras, IN; [2]Punjab Engineering College, IN

Abstract: *We present a robotic embedded system which learns wisely through human gestures. The robot uses using the Microsoft Kinect sensor along with the OpenNI libraries to recognize humans and approximate them with a skeleton. The positions of the joints of the skeleton are constantly monitored (shoulders, neck, wrist, elbow, hip, knee etc). Using these positions we recognize gestures. A simple pointing gesture would mean the shoulder, elbow and wrist are roughly aligned in a straight line. By extending this straight line, we can identify the object being pointed at. Similarly several other gestures can be recognized. The robots learn using the Reinforcement Learning paradigm combined with Markov Logic Networks. We used Robot Operating System (ROS) as the backbone for our framework's implementation and the robot control. The arm was controlled using OpenRave and an Arduino board. The robot currently does not respond to audio, although our framework can be extended to do the same. This is one of the things that we are currently working on. All that the robot needs is instructions in some form that it can understand. We restrict our robot currently to gestural instructions.*

HIPER-NIRGAM: A TOOL CHAIN BASED FRAMEWORK FOR MODELING THERMAL-AWARE RELIABILITY ESTIMATION IN 2D MESH NOCS

Ashish Sharma[1], Manoj Singh Gaur[1], Lava Bhargava[1], Vijay Laxmi[1] and Mark Zwolinski[2]
[1]Malaviya National Institute of Technology, Jaipur, IN; [2]University of Southampton, GB

Abstract: *Every three years, power density in system-on-chip (SoCs) gets doubled. As the semiconductor technology is scaling, the number of cores and interconnect network connections are increasing. To improve system performance while meeting permissible power limits, Chip-Multi Processors (CMPs) and many-core processors have emerged as an appealing solution. One of the significant aspects of many-core design is an on chip interconnect network that can effectively support intra-core and inter-core communications. This interconnect should be scalable, support high communication bandwidth and multiple concurrent connections among cores. Network-on-chip (NoC) replaces the traditional bus based interconnect architecture as former is scalable, has higher bandwidth, fault tolerance and offers parallelism. Regular NoC topologies improve scalability too. Adaptive NoC routing solutions distribute power densities and delay onset of hotspot creation. With ever-growing demand of computation and communication bandwidth by applications, the system designer need to consider and address resultant power and thermal issues in SoC as well as NoC design. Design tools need to incorporate thermal effects in design and evaluation of prototypes. Abstract--- Regional temperature differential and hotspots are two thermal problems in network-on-chip. On-chip thermal problems have an adverse impact on system performance and reliability. We propose creation of a toolchain based framework for incorporating thermal evaluation of NoC through existing simulation tools. Our proposed framework provides an integration of NoC simulator with power and thermal simulation models for analyzing the thermal hotspots and can be used for thermal-aware reliability estimation. In our framework, reliability estimation is based on life time failure models such as TDDB (Time dependent dielectric breakdown), NBTI (Negative bias temperature instability) and SM (Stress Migration). In our proposed reliability measurement is based on MTTF (Mean time to failure) comparative value. Our tool chain consists NIRGAM as a NoC simulator, NoC configuration parameters such as number of virtual channel, buffer size, routing logic, simulation cycles and application traffic are passed to power models (Orion 2.0 and McPAT). Power models provide the power trace and area of given NoC configuration. The power model results are further used in Hotspot 5.02 [HOTSPOT] thermal simulation model for generating floorplan and temperature trace (steady temperature file). The steady temperature trace used in reliability estimation tool REST [REST_tool] to estimating MTTF vales. Abstract--- We believe that this generic framework can be used by researchers on academia and industry to incorporate thermal-aware reliability estimation in their design exploration.*

ID.FIX: AN EDA TOOL FOR FIXED-POINT REFINEMENT OF EMBEDDED SYSTEMS

Olivier Sentieys[1], Daniel Menard[2] and Nicolas Simon[1]
[1]INRIA, FR; [2]INSA Rennes, FR

Abstract: *Most of digital image and signal processing algorithms are implemented into architectures based on fixed-point arithmetic to satisfy cost and power consumption constraints associated with most of embedded and cyber-physical systems. The fixed-point conversion process (or refinement) is crucial for reducing the time-to-market and design tools to automate this phase and to explore the design space are still lacking. The ID.Fix EDA tool, based on the compiler infrastructure GECOS, allows for the conversion of a floating-point C source code into a C code using fixed-point data types. The data word-lengths are optimized by minimizing the implementation cost under accuracy constraint. To achieve low optimization time, an analytical approach is used to evaluate the fixed-point computation accuracy. This approach is valid for systems made-up of any smooth arithmetic operations. Commercial tools can then be used to synthesize the*

architecture or to perform software compilation from the output fixed-point description of the application. Thus, the goal is to bridge the gap between the floating-point description developed by algorithm designer and the fixed-point description use as input for high-level synthesis or compilation tools.

IMPLEMENTATIONS OF THE SEMI-GLOBAL MATCHING 3D VISION ALGORITHM FOR AUTOMOTIVE APPLICATIONS

Affaq Qamar and Luciano Lavagno, Politecnico di Torino, IT

Abstract: *The demo will show our real-time hardware implementations on a Xilinx® ZynqTM System-on-Chip of the Semi-Global Matching (SGM) algorithm, which is frequently used in stereo vision systems, e.g. for automotive applications. We will also compare the quality of results, flexibility and design time that we achieved using both High-Level Synthesis (HLS) and manual RTL design. The use of HLS is particularly promising because the automotive industry is very sensitive to production costs, hence it requires various implementations of the same algorithm, with very different resolutions, costs, and performance levels, for different target market segments. SGM mainly consists of three sequential processing steps which are, (i) cost cube calculation, (ii) path cost computation and (iii) disparity estimation and minimization. The path cost computation further involves processing of pixel wise cost cube data into eight distinct directions. The initial algorithmic "golden" model used very large arrays, which had to be mapped to an external DRAM and brought into the on-chip RAM of the FPGA on demand. This required both adding the memory transfer loops and inserting calls to the AXI transactors that access the DRAM through the on-chip DDR slave. Moreover, the initial single-threaded algorithm had to be parallelized, by converting the top-level sweeps of the image in eight directions into forward and backward passes. Both manual RTL and HLS designs were suitable to achieve the target real-time performance. The design space was thus explored by making several fairly different micro-architectural choices. In the end, it was possible to obtain an implementation which is comparable to the manual RTL design. The authors intend to demonstrate the FPGA based HW implementation of the SGM algorithm (upon permission from the industrial partners) and discuss the HLS flow and comparison strategy.*

INTERACTIVE VISUALIZATION OF ESL DESIGNS

Jannis Stoppe[1], Robert Wille[2] and Rolf Drechsler[2]
[1]University of Bremen, DE; [2]University of Bremen/DFKI GmbH, DE

Abstract: *In this work, we propose an improved visualization tool for SystemC which assists a designer in communicating a system's structure and behavior. Please see the uploaded pdf-file for details.*

ISIS: CUSTOMIZABLE RUNTIME VERIFICATION OF HARDWARE/SOFTWARE VIRTUAL PLATFORMS

Laurence PIERRE and Martial Chabot, TIMA, FR

Abstract: *Debugging today's hardware/software embedded systems is a complex process. We have previously described our tool, ISIS, that enables the runtime Assertion-Based Verification (ABV) of temporal requirements for high-level (SystemC TLM) models of such systems. We present here an extended version of the tool, that gives the user the possibility to customize and to optimize the verification process.*

ISP RAS VERIFICATION TOOLS: INTEGRATED APPROACH TO HARDWARE VERIFICATION AT UNIT AND SYSTEM LEVELS BASED ON STATIC AND DYNAMIC METHODS

Andrei Tatarnikov, Mikhail Chupilko, Alexander Kamkin, Artem Kotsynyak and Sergey Smolov, Institute for System Programming of the Russian Academy of Sciences (ISP RAS), RU

Abstract: *Verification has long been recognized as an integral part of the hardware design process. As each hardware design is developed from unit- and core-level point of view, verification process should account this fact and provide means for dealing with both of them. Applied approaches include both static (formal methods, source code analysis) and dynamic (testing) methods. To facilitate verification, it is important to provide a uniform methodology that would allow integrating different approaches. In this work, we present a set of verification tools that takes advantage exactly of combining static and dynamic approaches. This allows knowledge sharing between tools, which helps to build more accurate models of hardware designs to be used in verification activities at different levels of abstraction. Brief descriptions of the tools are given below. MicroTESK is a reconfigurable (retargetable and extendable) model-based test program generator for microprocessors and other programmable devices. Lightweight formal specifications customize the generator for a particular architecture and provide knowledge about situations to be covered by tests. A convenient test template framework allows rapid development of complex verification scenarios. Being retargetable, MicroTESK is able to support various RISC and CISC architectures. C++TESK is an open-source C++ based toolkit intended for automated functional testing of software components (mostly in C/C++) and RTL (HDL) models of digital hardware (in Verilog and VHDL). The main part of the toolkit is a library of C++ classes and macros that define facilities for constructing formal specifications (reference models), adapters of components under test, test scenarios and test coverage metrics. Basing on C++ descriptions provided by a user, a test system is compiled. It allows automatically generating and applying sequences of stimuli to the component under test, checking correctness of its reactions and collecting statistics on test execution. Besides the basic library, the toolkit includes a report generator, means for parallelizing test execution on*

computer clusters, and Eclipse-based IDE. The toolkit is planned to be integrated into UVM methodology. Retrascope is an extendable toolkit for RTL (HDL) models transformation and functional verification at unit level. Analyzing source HDL-code, it extracts control and data flows, transforms them into Extended Finite State Machines (EFSM), and generates covering test sequences for them. The toolkit supports RTL modules written in VHDL and Verilog. It can be used both from command line and from Eclipse-based IDE.

LINUX ON TSAR: PORTING THE LINUX KERNEL TO THE TSAR MANYCORE ARCHITECTURE

César Fuguet Tortolero, Joël Porquet and Alain Greiner, UPMC-LIP6, FR

Abstract: *In this demonstration, we explain how we ported a Linux-based Operating System to the TSAR manycore architecture. In the associated poster, we describe the TSAR architecture and enumerate the pieces of software that usually need to be ported for a new processor architecture, and we give further details about our port. We also demonstrate this work by running Linux on a FPGA-based prototype of TSAR. The demo shows the entire boot process, from the powerup to the terminal prompt where the user can type in commands and interact with the hardware system.*

MAMMA: SPEECH ENHANCEMENT DEMO EXPLOITING MEMS MICROPHONE ARRAY FOR PEOPLE WITH DISABILITIES

Luca Fanucci[1], Alessandro Palla[1] and Roberto Sannino[2]
[1]University of Pisa, IT; [2]STMicroelectronics, IT

Abstract: *Disabled people, especially the ones with motor skill impairments, have difficulties in interaction with electronic devices. Indeed voice recognition could be exploited, but its performance strongly depends by the environmental noise. We propose a wearable speech enhancement system based on MEMS microphone array and an ARM Cortex M4 CPU featuring a beamforming technique and an adaptive acoustic echo cancellation filtering in order to increase SNR of acquired voice stream. An increase by 16.5 dB in the SNR is obtained when noise and voice come from opposite directions. Theoretical analysis and in-system measurements prove the effectiveness of the proposed solution.*

NETFPGA SUME: NETFPGA SUME: MAKING 100GBPS A COMMODITY

Noa Zilberman, Yury Audzevich, Georgina Kalogeridou and Andrew W. Moore, University of Cambridge, UK

Abstract: *The demand-led growth of datacenter networks has meant that many constituent technologies are beyond the budget of the wider community. In order to make and validate timely and relevant new contributions, the wider community requires accessible evaluation, experimentation and demonstration environments with specification comparable to the subsystems of the most massive datacenter networks. We will demonstrate NetFPGA SUME, an open-source FPGA-based PCIe board with I/O capabilities for 100Gbps operation as NIC, multiport switch, firewall, or test/measurement environment.*

NUMERICAL METHODS FOR EFFICIENT SIMULATIONS OF CIRCUITS WITH SEPARATED TIME SCALES

Genie Hsieh, Sandia National Laboratories, US

Abstract: *Circuit simulations can support to analyze and predict the performance, safety, and reliability of nuclear weapons and to certify their functionality. Small circuits with strong, nonlinear oscillations (i.e. circuits have separated fast/slow time scales; hereafter denoted by "fast/slow circuits") can make the computation time of even a single simulation unmanageable. These types of circuits are common in weapon systems. Many numerical methods are proposed to speedup such simulations by utilizing multiple time variables to efficiently represent circuit signals with widely separated rates of variation. However, weapon circuits possess complex behaviors that are shown to be the outstanding challenges in this research field. In this work, we develop novel numerical methods for fast/slow weapon circuit simulations and deliver significant simulation speedups to facilitate efficient weapon assurance.*

ODEN: ASSERTION MINING FOR BEHAVIORAL DESCRIPTIONS

Alessandro Danese, Alessandro Danese, Tara Ghasempouri and Graziano Pravadelli, University of Verona, IT

Abstract: *Specification mining is an automatic approach for extracting assertions from the implementation of the system under verification (SUV). Its primary goal is to improve the verification and documentation process by making available a matching between a manual definition of the expected functionality and a formalization of the actual implemented functionality. In order to automatically extract assertions, some approaches perform a static analysis of the SUV source code. These solutions, despite of their effectiveness, suffer of scalability problems. To overcome this drawback, dynamic approaches have been also proposed that extract assertions by relying only on the observation of SUV's execution traces. This guarantees a better scalability, even if only "likely true assertions" can be extracted. For this reason a qualification phase is generally implemented in order to discard irrelevant and spurious assertions. In this context, ODEN is a tool for dynamically extracting likely true assertions by combining static and dynamic techniques. ODEN works with both hardware design and software applications. The tools analyses the execution traces of the system under verification and it generates assertions in the form of temporal relationships between arithmetic/logic expressions over the variables of the SUV. With respect to existing tools, ODEN works on a wider range of abstraction levels (e.g., gate-level, RTL, TLM, SW level, ...) and it considers a wider set of temporal patterns to more precisely characterize the behaviours of the SUV.*

ORIENTOMA: A WEARABLE ORIENTATION SYSTEM FOR BLIND AND VISUALLY IMPAIRED PEOPLE

Giuseppe AiroFarulla, Marco Indaco and Ludovico Russo, Politecnico di Torino, IT

Abstract: *This work aims to design and implement a low-cost wear-able orientation system able to help blind (or visually im-paired) people to walk and orienting autonomously in un-known environments. The basic principle is to create a system able to understand information from the context where the user is and to convey such information using a way that is intelligible for blind people. Such information may come from suitable sensors integrated in the user's smartphone, which represents the core of the system, and/or from other wearable devices each people is sup-posed to have, such as a smartwatch.*

OSTC: COMBINING HIFSUITE AND SCNSL FOR SMART DEVICE INTEGRATION AND SIMULATION

Graziano Pravadelli, Alessandro Danese, Franco Fummi, Valerio Guarnieri, Michele Lora, Graziano Pravadelli and Francesco Stefanni, University of Verona, IT

Abstract: *The main design issue of smart devices is their high degree of heterogeneity, due to the simultaneous presence of multiple domains and extra-functional properties, together with the traditional system functionality. This makes design and simulation very challenging, even because heterogeneity implies that the functionality is not the only dimension that must be considered at validation time. Other properties, such as power consumption or thermal dissipation, are critical to ensure correctness of the final product and to correctly estimate its behavior. This makes component integration and simulation key phases in the design and verification process of smart devices. Thus, to efficiently master smart device design, it is fundamental to be aware of design issues and to know how to solve them through innovative tools and methods, which allow integrating all the components of a smart device into an efficient and flexible simulation platform. We addressed such issues by means of the combined use of HIFSuite tools and SCNSL to obtain a homogeneous and fast SystemC/C++ model of a smart device through the compositions of heterogeneous components. An Open Source Test Case (OSTC) has been defined to show the potentiality of the proposed methods and tools.*

PARLOMA: A REMOTE COMMUNICATION SYSTEM FOR DEAFBLIND PEOPLE

Ludovico Orlando Russo[1], Giuseppe Airò Farulla[1], Marco Indaco[1], Calogero Maria Oddo[2], Daniele Pianu[3], Paolo Prinetto[1], Stefano Rosa[1] and Ludovico Orlando Russo[1]

[1]Politecnico di Torino, IT; [2]Scuola Superiore Sant'Anna, The Biorobotics Institute, IT; [3]CNR, IEIIT, IT

Abstract: *This work aims at designing a low-cost communication system to allow remote communication among deafblind people, up to now impossible. Due to their lacking of both the auditory and the visive channel, deafblind people can receive feedbacks and mes-sages only resorting on hand-in-hand communication and only from speakers physically located near them. Such limitation ag-gravates their situation and cause deafblind people to live behind a wall of isolation from active society. PARLOMA aims at breaking this wall, developing a tool that can be used by deafblind people to communicate whenever they want and wherever they are.*

REAL-TIME MULTIPROCESSOR COMPILER DEMO: COMPILER FOR REAL-TIME MULTIPROCESSOR SYSTEMS WITH SHARED ACCELERATORS

Bekooij Marco, Guus Kuiper, Stefan Geuns, Philip Wilmanns, Joost Hausmans and Marco Bekooij, University of Twente, NL

Abstract: *Accelerators are added in real-time multiprocessor systems for power-efficiency improvement and cost reduction. Sharing of these accelerators improves their utilization but without tool support it also complicates programming. This demonstration shows a multiprocessor compiler for a real-time multiprocessor system that contains support for the sharing of hardware accelerators. The capabilities of this compiler are demonstrated by mapping a packet based GMSK receiver application onto this multiprocessor system. The multiprocessor system is implemented on a Xilinx Virtex-6 FPGA to which an RF front-end is connected. This multiprocessor system contains 16 Microblaze processors and 5 accelerators. With this system a real-time digital audio stream is received and demodulated.*

REAL-TIME PATTERN DETECTION OF MOVEMENT RELATED POTENTIALS BY SYNCHRONIZED EEG AND EMG

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Abstract: *Before the conscious intention to perform any voluntary movement, our brain has already activated the action, 1s before the muscle activity actually starts. The brain processes are necessary to determine the performance of the movement itself. The presence of both the premotor potential (also called "Bereitschaftspotential" or "Readiness Potential" in the 2-5 Hz band) and the Mu-rhythm (in the 7-12 Hz) is particularly interesting for the detection of voluntary movement. Therefore, the detection of these movements' related potentials (MRPs), before the EMG activation, indicates the movement intentionality. Due to the presence of artifacts (blinking, eye movement, swallowing etc.) that spoil EEG signals, the real-time detection of MRPs is particularly challenging. In this proposal, we describe a complete wearable system performing synchronous EEG and EMG monitoring to on-line detect MRPs and prevent unintentional and dangerous movements. The Bereitschaftspotential (BP) and Mu-rhythm detection is carried out through a wavelet analysis on differential signals captured 1-second before the EMG activation. This differential approach allows discerning*

if the recorded EEG activity is related to the motor cortex or if it is just a common artifact. The EEG/EMG monitoring system can face the strict requirements of ambient assisted living application (AAL), taking care of aged and disable people in a domestic environment. Specifically for this application, the system can be configured as following: data from 12 EEG channels are firstly collected in a central unit that wirelessly communicates with the gateway (24 bit resolution – 500 Hz sampling rate), the gateway receives data also from each of the 8 EMG nodes (12-bit resolution, 500 Hz sampling rate). For a comfortably use, a battery life of – at least – 10 hours, have to be implemented. Moreover, a working range of 10 meters (between nodes and gateway) is considered. Above all, the requirement of wearability is achieved by the transfer printing technology, produced using photolithography and dry etch techniques, that allows the creation of wireless, tiny and lightweight electrodes for both EEG and EMG printed on bio-polymers (Polycaprolactone). Since a huge amount of retrieved data is expected, a data rate of 250 kbps (~31 kBps) is needed: a good compromise in terms of power consumption and data rate is achieved through the standard IEEE- 802.15.1 (Bluetooth low energy –BLE). The gateway unit (a smartphone or a tabled) receives the EEG and EMG sensor data and performs signal analysis to identify possible MRPs patterns through wavelet analysis. In this contribute it will be delineated as case study the possible implementation in fall prevention where not only the unwanted muscle movement is detected but also a bio-feedback is activated to block the muscle and inform an assistive center. Nevertheless, the field of application of the system here presented covers a wide range of AAL applications including fall prevention, rehabilitation (i.e. walk monitoring), artificial limb control and neurodegenerative diseases diagnosis.

RECONFIGURABLE FPGA-BASED NON-INTRUSIVE BERT FOR PRODUCTION TEST

Sergei Odintsov and Artjom Jasnetski, Tallinn University of Technology, EE

Abstract: *We introduce an FPGA-based Bit Error Rate (BER) tester solution for high-speed serial links targeting production environment. This solution does not require usage of external T&M equipment or extra DFT. As opposed to intrusive physical probing with external BER tester our approach produces more relevant output because measurement is done using transceivers in their functional mode. Introduced BERT instrument supports fine tuning of link parameters and pattern generation. This solution can replace long lasting BER test by quick evaluation of link quality using eye diagram.*

RSOC FRAMEWORK: FRAMEWORK FOR RAPID PROTOTYPING OF APPLICATIONS ON RECONFIGURABLE SOCS

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Abstract: *Recent chips with ARM based processors and FPGA logic provide potential for many applications. IP cores and operating systems (OS) have been prepared to simplify development. However the integration of IP cores and OS is not covered by any development tool yet. We propose universal Reconfigurable System on Chip (RSoC) Framework to support rapid prototyping of different applications on these chips. Application can run in FPGA and/or in processor and RSoC Framework covers all mutual communication.*

SMART CELL DEVELOPMENT PLATFORM FOR EMBEDDED BATTERY MANAGEMENT

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Abstract: *Embedded Battery Management (EBM) [1], in contrast to the existing state-of-the-art centralized Battery Management Systems (BMSs) found in Electric Vehicles (EVs) or stationary Electrical Energy Storage (EES) applications, focuses on monitoring and controlling each individual cell of the battery pack with a dedicated Cell Management Unit (CMU). This novel approach of battery management might offer significant advantages over the centralized BMSs, such as higher modularity, plug-and-play integration and shorter time to market. The combination of a battery cell and a CMU forms the smart cell and the system-level functionalities of the EBM are performed in a decentralized manner by the network of smart cells, with the help of the computational and communication resources of CMUs. We present a development platform for such a smart cell enabled EBM. The development platform consists of two components, the hardware platform and the software platform. The hardware platform of the demonstrator comprises of battery cells and their dedicated CMUs which consist of a smart cell controller board and an active cell balancing board. The software platform provides the smart cell firmware as well as a software tool for verification of active cell balancing architectures and a smart cell simulator for simulating system-level EBM functionalities.*

STRNG: A SELF-TIMED RING BASED TRUE RANDOM NUMBER GENERATOR WITH MONITORING AND ENTROPY ASSESSMENT

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Abstract: *The Self-timed ring based True Random Number Generator (STRNG) leverages the jitter of events propagating in a self-timed ring to generate provably random binary sequences. Several implementations in FPGAs and in CMOS design flows have shown the feasability of this generator in digital technologies, and also confirmed that it can provide high quality random bit sequences that pass the standard statistical test batteries at rates as high as 200 Mbit/s. Following AIS31 recommandations for the design and evaluation of TRNGs, the security of this generator is based primarily on an entropy assessment obtained by modeling the entropy extraction and measuring the entropy source.*

Secondly, the generator is protected against active attacks by monitoring its behavior in real-time or on demand. In this demonstration, we illustrate this approach in an Altera Cyclone III implementation of the STRNG. We show how the design is configurated depending on the measurement of the entropy source (the jitter magnitude) in order to guarantee a given minimum entropy rate per output bit. Then, we emulate physical attacks on the generator by willingly manipulating its internal structure in order to demonstrate how the entropy monitoring can detect abnormal behaviors and send the appropriate alarms.

SYSTEM-LEVEL FPGA PROTOTYPING OF ANALOG/MIXED-SIGNAL SYSTEMS

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Abstract: *System-level verification of large-scale mixed-signal systems using virtual prototypes is a powerful tool for design and verification. Still, the limited computing power demands for new methods to enhance the simulation performance. For digital hardware development FPGA-based prototyping is commonly used to enable faster verification of hardware and software system-components. We focus on a new approach for embedding system-level analog/mixed-signal models in FPGA-based verification environments. Starting from a system-level SystemC description of an A/MS circuit, we synthesize a model-specific FPGA-based hardware accelerator capable of running A/MS simulations using floating-point data types. This new approach will be demonstrated by prototyping an A/MS pressure-sensor frontend ASIC on an FPGA board.*

THE Ψ-CHART DESIGN APPROACH IN TTOOL/DIPLODOCUS: A FRAMEWORK FOR HW/SW CO-DESIGN OF DATA-DOMINATED SYSTEMS-ON-CHIP

Andrea Enrici, Ludovic Apvrille, Daniel Camara and Renaud Pacalet, Télécom ParisTech, FR

Abstract: *In the scope of the DATE 2015 University Booth, we present our latest achievements for the system level design of parallel and distributed embedded systems. We propose a demonstration of a novel design approach, the Ψ-chart, in TTool/DIPLODOCUS, a UML/SysML framework for the design, validation and automatic code generation for data-dominated SoCs. The Ψ-chart is a design approach where communication patterns are designed with dedicated models, independently of a pair application-architecture, before mapping phase. It allows for a complete orthogonalization of concerns between the design of computations and communications, thus achieving faster Design Space Exploration, complete design portability as well as reduced design times and costs. The subject of our demonstration is the design of the physical layer (PHY) of the transmitter part of the Zigbee wireless standard (IEEE 802.15.4) mapped onto a MPSoC architecture with shared memory. Our demonstration will illustrate the full design of the Zigbee transmitter, from models to the automatic generation of the emulation code, via simulation and formal verification. We will validate our design by comparing the output samples produced by the emulation code, with a real implementation of the transmitter on a FPGA prototyping board.*

VDA-ADMF: AN AGILE MIGRATION FRAMEWORK FOR ANALOG LAYOUT DESIGN

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Abstract: *Layout generation in the late analog CMOS design is challenging by its increasing layout constraints and performance requirements. However, iterative refinement on manual design damages the productivity of analog layout. Therefore, it is more efficient to enroll the know-how from existing design instead of generating a new one. To contend with time-consuming analog layout for more possibilities, this software aims to demonstrate a fast layout prototyping framework for migration purpose into real layout design. In our framework, a reference analog layout design is given to generate potential layout candidates at the objective technology. The demonstration includes the original layout, the extracted topology with placement and routing, the generated layout figures, the dumped layout results and the simulated results. This procedure of migration provides a convincing exhibition of our migration framework.*

VHDL TO SYSTEMC TRANSLATION AND ABSTRACTION: SYSTEMC MANIPULATION FRAMEWORK: FROM RTL VHDL TO OPTIMIZED TLM SYSTEMC

Syed Saif Abrar, Syed Saif Abrar, Valentin Tihhomirov, Maksim Jenihhin and Jaan Raik, Tallinn University of Technology, EE

Abstract: *We propose a novel framework for SystemC manipulation based on the open-source hardware design and analysis environment zamiaCAD. The framework provides for optimized VHDL-to-SystemC translation and subsequent abstraction to higher-levels. It includes an Eclipse-based front-end and is integrated to a comprehensive environment for RTL VHDL analysis, simulation and debug.*

WHERE IS IT? FIND THE CODE YOU ARE INTERESTED IN!

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Abstract: *The demonstration presents our tool for feature localization and debugging of RTL-designs. Feature localization*

helps a designer to find the code relevant for a certain feature and, thus, helps him to faster understand a design previously unknown to him. The developer can choose between three basic techniques for feature localization. In the area of debugging the tools allows fault localization, reverse debugging based on dynamic data- and control-flow of the design and dynamic slicing.

WORKCRAFT: WORKCRAFT: FRAMEWORK FOR INTERPRETED GRAPHS

Danil Sokolov, Newcastle University, GB

Abstract: *Workcraft is a cross-platform framework for capture, simulation, synthesis and verification of graph models. It supports a wide range of popular graph formalisms and provides a plugin-based framework for modelling and analysis of new model types.*

XTSI: THE 3-D ELECTRO-THERMAL SIMULATOR

Jürgen Scheible and Carl Christoph Jung, Reutlingen University, DE

Abstract: *xtSi is a 3D electro-thermal simulation tool for integrated circuits. It uses a computationally efficient algorithm, which allows the simulation of typical ICs in only a few minutes. The temperature distribution is depicted graphically and with temporal resolution in a specially designed graphical user interface. With the help of xtSi designers can exactly identify isotherms and hotspots, thus enabling an optimization of the layout due to temperature effects. xtSi has been verified experimentally for device temperatures exceeding 500 °C up to the onset of thermal runaway.*

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