This demonstration presents a floorplanner tool addressing partially-reconfigurable FPGAs. The input of the tool consists of a set of regions described in terms of their heterogeneous resource requirements together with the number of interconnections among regions and the target FPGA of the partial reconfiguration (PR) design.

Once the input are specified, the floorplanner allow the designer to manually or automatically perform the floorplan of the regions. If the regions are floorplanned manually, then, the user receive feedbacks on the validity of the solution and can quickly modify the shape and positions of the regions to achieve feasible solutions. Invalid solutions arise if two reconfigurable regions overlap, or a reconfigurable region cover an area of the device that cannot be used for partial reconfiguration (such as areas assigned to static logic or hard processors), or if the resource requirements of the regions are not meet in the current configuration.

The designer can also require the tool to perform an automatic floorplan optimization to find a good feasible solution for the current regions requirements. In this scenario, three cost metrics linearly combined in a global objective function are used to determine the quality of the solutions. Specifically, the tool consider the overall wire length between reconfigurable regions, the overall number of wasted resources and the perimeter of the regions (minimization of the perimeter on a fixed area can lead to better aspect ratios suitable for the subsequent place and route stage). The designer can select to what extent consider each of the cost metrics depending on his/her needs, moreover, regarding resource wasted, it is possible to assign a cost to each different type of resource. The minimization of the objective function is performed exploiting a Mixed-Integer Linear Programming (MILP) formulation that can be solved to optimality when enough time is given. If the designer has already found a feasible solution, the starting floorplan is used to warm start the solver and speed-up the optimization process.

In this demonstration, to enhance the user experience, we limited the execution time of the solver to 5 seconds and we fixed the number of reconfigurable regions to 4. Since a limited time budget is given to the solver the optimality of the solution with respect to the user defined objective function is not guaranteed, but in general, good results can be achieved. The FPGA considered for the demonstration is a Xilinx Virtex-5 XC5VLX110T, a heterogeneous device that allow regions to reconfigure different resources such as CLBs, DSPs and BRAMs. The user can set his/her own preference on the objective function, is allowed to define the resource requirements of the regions and the number of interconnections between them.

The tool is online at floorplacer.necst.it.