An Agile Migration Framework for Analog Layout Design

Po-Cheng Pan*, Prof. Hung-Ming Chen*

*Institute of Electronics and SoC Center, National Chiao Tung University, Hsinchu, Taiwan
Email: benbean.ee96g@g2.nctu.edu.tw; hmchen@mail.nctu.edu.tw

Abstract—Layout generation in the late analog CMOS design is challenging by its increasing layout constraints and performance requirements. However, iterative refinement on manual design damages the productivity of analog layout. Therefore, it is more efficient to enroll the know-how from existing design instead of generating a new one. To contend with time-consuming analog layout for more possibilities, this software aims to demonstrate a fast layout prototyping framework for migration purpose into real layout design.

In our framework, a reference analog layout design is given to generate potential layout candidates at the objective technology. The demonstration includes the original layout, the extracted topology with placement and routing, the generated layout figures, the dumped layout results and the simulated results. This procedure of migration provides a convincing exhibition of our migration framework.

I. BACKGROUND AND RELATED WORK

The application of analog layout generation is widely developed in academia and industry. Commercial tools like Cadence Virtuoso ADE, Synopsys Laker have provided template-based schematic-driven analog layout generator. However, the generated layout mostly keeps the original topology. Our software integrates mechanisms from [1], [2], [3]. The device sizes of targeting technology is generated from [3]. In [1], it provides multiple placement results withholding analog layout constraints. For routing generation, [2] preserves the behavior of routing from the reference layout and fast generates routing on the targeting layout.

II. FLOW OF OUR FRAMEWORK

In order to provide fast prototyping for layout migration, this software extracted the reference layout with placement and routing respectively. The migrated layout is generated according to the extracted information, and then it dumps into real design after physical verification for performance simulation. Fig. 1 shows the overall flow diagram of our methodology. The flow is mainly separated into three stages:

1) Extraction and Preservation: A layout extraction and preservation technique [2] can not only be applied to generalized layout, but also hierarchical design.

2) Prototyping: The preserved topology of original layout can be generated into multiple layout candidates with placement and routing.

3) Wire optimization: A detailed routing refinement is applied automatically to route the unrouted nets for final verification and simulation.

In the end, a set of layouts with refinement is obtained, which provides designers a quick look of possible solutions that can be used. The layout results are automatically dumped into industrial layouts for demonstration and simulation.

III. PROGRAM SETTING AND RESULTS

Our Software is developed with g++ 4.1.2 for methodology, Synopsys PyCell Studio™ 4.7.1 for layout realization and Qt 4.8.4 for GUI demonstration. We also display the layout with the reference one and the generated layout via Cadence® Virtuoso® 6.1.5. The migration of a variable-gain amplifier (VGA), a folded-cascode operational amplifier (OpAmp) and low dropout regulator (LDO) will be demonstrated step-by-step as applications to show the feasibility of our Software.

REFERENCES

