RSoC Framework utilized to speed up video processing on ZedBoard

Video processing applications often require hardware acceleration to reduce processor load and power consumption. Xilinx Zynq consist of the ARM Cortex-A9 and the FPGA logic for hardware acceleration. Therefore it is a perfect platform to implement embedded video processing solution. In this demonstration the time-critical task of video noise filtering (by 3x3 median filter) is implemented:

1. as a standard program for ARM processor,
2. using intrinsic functions for ARM NEON and
3. as an acceleration engine in the FPGA logic.

In all cases, ARM processor is utilized to control the video stream. The user application running in Linux loads a video file from the local flash storage. This noisy video stream is processed by (1) ARM processor, (2) ARM NEON engine or (3) sent to the engine implemented in FPGA. The RSoC Framework is utilized to achieve high throughput between ARM and FPGA logic and to simplify design process. There is no need for interconnections, DMA engine instantiation or driver development with use of RSoC Framework.

The processing (1,2 or 3) depends on the external button and it is also indicated on ZedBoard's integrated OLED display. External button is handled by GPIO core (Xilinx XPS General Purpose IO). The GPIO can be connected either to RSoC Bridge or to the ARM directly. If the button is pushed, an interrupt is triggered to ARM to set up one of three types of processing or just send unfiltered video to the output. The video stream is forwarded to HDMI controller core which is implemented in the FPGA logic and displays the video on the monitor. Therefore it is possible to demonstrate the speed of image processing in three different implementations.

This video processing application has been prototyped rapidly with the RSoC Framework. More information about RSoC Framework and this demo are available at: www.rsoc-framework.com