FPGA-based Hardware Acceleration of Analog/Mixed-Signal SystemC Models

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Abstract—System-level verification of large-scale mixed-signal systems using virtual prototypes is a powerful tool for design and verification. Still, the limited computing power demands for new methods to enhance the simulation performance. For digital hardware development FPGA-based prototyping is commonly used to enable faster verification of hardware and software system-components. We focus on a new approach for embedding system-level analog/mixed-signal (A/MS) models in FPGA-based verification environments. Starting from a system-level SystemC description of an A/MS circuit, we synthesize a model-specific FPGA-based hardware accelerator capable of executing A/MS model-code using floating-point data types.

This new approach will be demonstrated by prototyping an A/MS pressure-sensor frontend ASIC on an FPGA board.

I. APPLICATION SCENARIO

Virtual prototyping of analog/mixed-signal (A/MS) systems is a key concern in the modern design process. Nevertheless, these simulations can not be embedded in a real-world test-environment as a hardware-in-the-loop (HiL) prototype due to the lack of simulation performance and the high effort of coupling an analog simulator to a HiL environment. In this application, we focus exemplary on the synthesized simulation of a sensor-frontend ASIC comprising an PWM modulator commonly used in smart-sensor systems as shown in fig. 1. To evaluate the performance of this system, characteristics such as non-linearity or temperature-dependence have to be simulated. These simulations require a significant amount of time for simulating e.g. DNL/INL in wide temperature ranges.

II. FPGA-BASED REAL-NUMBER SIMULATION

For simulating the regarded system modeled in SystemC[1] with sufficient accuracy in the targeted FPGA environment it is necessary to realize the calculations in an appropriate way. Therefore, we use a user-defined synthesizable floating-point datatype that can be adapted to the accuracy needs for modeling the components. These datatypes allow a real-like modeling scheme to synthesize event-driven mixed-signal simulations in an FPGA using the Cadence C-to-Silicon Compiler[2].

III. CONCLUSION

In this contribution, we demonstrate the possibility of FPGA-based prototypes of A/MS systems based on a synthesized SystemC model. These prototypes can be easily applied to common HiL test-environments to enhance mixed-signal verification scenarios.

ACKNOWLEDGMENT

This work has been carried out in the project ANCONA, funded by the German Federal Ministry of Education and Research (BMBF) in the ICT2020 program under grant no. 16ES021. The demonstrator is based on data taken from the project HoTSens (BMBF grant no. 16ES0008).

REFERENCES


Fig. 1. Architecture of demonstrator: The prototype of the sensor interface is realized inside a synthesized simulator attached to a second FPGA used for development of the signal processing system.