A Framework for the Emulation and Prototyping of Nano-Photonic Optical Accelerators

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Introduction

The recent advances in on-chip optical communication anticipate nano-photonic optical computing as a disruptive new technology. Different architectural solutions and competing physical implementations are currently being investigated. They include a wide spectrum of approaches such as those based on optical analog processing (e.g., nano-photonic optical vector–matrix multiplication [1]), digital optical gates (e.g., reversible nano-photonic gates [2], BDD-based approaches, etc) or even quantum computing [3]. Since the computing, performance, and error characteristics of these technologies differ substantially from those of standard CMOS technologies, an early co-design framework for nano-photonic accelerators embedded with digital multiprocessor systems is urgently required. It should allow an early investigation about the possible implementation of some kernels using optical accelerators and the effect of optical non-idealities in the overall system.

This demo presents a framework for the virtual emulation and prototyping of nano-photonic accelerators for optical analog processing and optical digital gates, currently being developed at the “Institute of Electrodynamics and Microelectronics” (ITEM) and at the “Bremen Institute for Applied Beam Technology” (BIAS). This framework, based on the ideas of rapid prototyping and virtual emulation using FPGA technology, provides two levels of operation. At a first level, it offers a library of models that can be used to construct a virtual prototype of a hybrid multi-processor and nano-photonic system. The parameterizable models emulate several optical non-idealities but are synthesizable at the RTL-level, so that a standard FPGA-emulation of the complete system can be carried out. In a second level, it offers the possibility to plug-in a macroscopic optical accelerator to prototype the nano-photonic one with higher accuracy.

In order to illustrate these two levels of operation, the demo at the DATE University-Booth will be twofold.

Virtual emulation demo

In the first demo, the user can define the functionality of the optical accelerator. Using a reversible–toolchain based on the RevKit [4] tools by the “Computer Architecture and Reliable Embedded Systems” (AGRA), a reversible implementation is created. The structural reversible implementation is transformed into a nano-photonic model which is emulated in a FPGA. The final system, composed by a standard processor communicating with the nano-photonic model of the accelerator, can be programmed in C so that the user can study the impact of the accelerator in its algorithm.

Physical prototype-demo

This demo focuses on the prototype of a low-cost vector–matrix multiplication core using optical processing. The optical prototype is composed by a sandwich of two LCD structures with orthogonal polarizations sending an image to an integrated camera. The different elements are controlled by a hardware–IP and connected to an embedded processor.

The user can define several parameters of the optical processor, such as the optical block size, the photodetector pitch etc. The physical prototype is then configured to that mode, and used as an optical accelerator by a microprocessor embedded in a FPGA. Again the user can program some C algorithms to study the system performance. Additionally a link to Matlab® allows the analysis of the precision achieved by the optical vector–matrix–multiplication process.

Bibliography