Alpexpo, Grenoble, France
Event 18 – 22 March
Exhibition 19 – 21 March
Design, Automation
& Test in Europe
The European System Design Show
From Systems-on-Chip to Embedded Computing
www.date-conference.com
The DATE organisation and sponsors would like to extend their warmest gratitude to all press journalists who give DATE coverage in the editorial pages. Listed below are the media houses and publications who generously agree to media partnership with DATE, and whose publications can be found at distribution points around the exhibition.

**CHIP DESIGN MAGAZINE**
Chip Design covers all of the technical challenges and implementation options engineers face in the development and manufacture of today’s complex integrated circuits. Chip Design is the only media network dedicated to the advanced IC Design market. Visit www.chipdesignmag.com to stay informed about the latest developments in chip modeling, architecture, design, test and manufacture, from EDA tools to digital and analog hardware issues. The System Level Design and Low Power Engineering Portals offer focused editorial content you won’t want to miss. And, be sure to visit www.http://eecatalog.com/ for valuable information about all of Extension Media’s outstanding technology resources.

**ELEKTRONIK I NORDEN**
Elektronik i Norden, an important tool for the Nordic electronic industry. We want Elektronik i Norden to be the most important source of information for the Nordic electronic industry (Sweden, Finland, Norway and Denmark). A circulation of 25 800 personally addressed copies proves we are the major electronics paper in this area. We publish news, comments and in-depth technical articles.

**EDA Confidential**
EDA is a commercial-free publication providing a quiet place for conversation about the Electronic Design Automation industry and its companion technologies. The coverage does not intend to be comprehensive, but does intend to provide some food for thought. To that end, EDA Confidential includes “Recipes”, Freddy Santamaria’s "Gourmet Corner", as well as "Voices" of other contributing authors, "Off the Record" op-ed pieces, and "Conference" coverage.

**ElectroniqueS**
ElectroniqueS is the reference monthly for decision makers and engineers in the electronics sector.

**The IET**
The IET is Europe’s largest professional body for engineers and technologists, we offer a wide range of products, services and professional qualifications to keep you ahead of the game. With 150,000 members based in 127 countries networking is key to their and your success - find out how to join and be part of the Knowledge Network by visiting us at our stand or visit www.thetiet.org

**vertical newsletter, 3 subjects: Automotive / Mil-Aero / Medical**
5 mailings a year (each 2 in 3 months)
Welcome to DATE 13

In this exhibition guide you will find listings of exhibitors contact details and their products being demonstrated on the exhibition floor. The classified product finder will help you locate the right solution within the show; maps and plans of Alpexpo and the exhibition hall will also help you to get around.

FREE - ENTRY to KEYNOTE SESSIONS, EXHIBITION THEATRE (see p.7) & SPECIAL EVENTS!

OPENING PLENARY KEYNOTES –
Tuesday, March 19, 2013, 0830 – 1030
Smart systems for internet of things
Benedetto Vigna - Executive VP of STMicroelectronics, IT
Creating a sustainable information and communication infrastructure
Massoud Pedram - Professor at University of Southern California, US

Exhibition Opening Times:
Tuesday 19 March 1000 - 1830*
(*Evening Reception from 1830 – 1930hrs)
Exhibition Drinks Reception offered by the City of Grenoble

Wednesday 20 March 1000 - 1800

Thursday 21 March 1000 - 1700

Entrance to the Exhibition is FREE
of such smart systems goes beyond the design of the individual components and subsystems and consists of accommodating a multitude of functionalities, technologies, and materials to play a key role to augment our daily life.

Since the first mobile computer, power efficiency was a key measure for success. As the need for performance ever increases, the energy cost of performance has metric well beyond just the life of the battery in mobile. Energy efficiency is now the driver in most consumer products, the compute density of a server, and has become the primary limit in the delivery of high performance. During this talk we will consider the various power related limitations of compute while discovering how the techniques and new capabilities introduced into mobile computing also bring the flexibility to address the limitations of the traditional computing approach.

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**Smart systems for internet of things**

Benedetto Vigna - Executive VP of STMicroelectronics, IT

Sensors add intelligence to systems which represent a broad class of devices incorporating functionalities like sensing, actuation, and control. They are the core of smart components and subsystems; then, the challenge in the realization of such smart systems goes beyond the design of the individual components and subsystems and consists of accommodating a multitude of functionalities, technologies, and materials to play a key role to augment our daily life.

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**Creating a sustainable information and communication infrastructure**

Massoud Pedram - Professor at University of Southern California, US

Modern society's dependence on information and communication infrastructure (ICI) is so deeply entrenched that it should be treated on par with other critical lifelines of our existence, such as water and electricity. As is the case with any true lifeline, ICI must be reliable, affordable, and sustainable. Meeting these requirements (especially sustainability) is a continued critical challenge, which will be the focus of my talk. More precisely, I will provide an overview of information and communication technology trends in light of various societal and environmental mandates followed by a review of technologies, systems, and hardware/software solutions required to create a sustainable ICI.

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**Energy efficient computing**

John Goodacre, ARM, UK

Since the first mobile computer, power efficiency was a key measure for success. As the need for performance ever increases, the energy cost of performance has metric well beyond just the life of the battery in mobile. Energy efficiency is now the driver in most consumer products, the compute density of a server, and has become the primary limit in the delivery of high performance. During this talk we will consider the various power related limitations of compute while discovering how the techniques and new capabilities introduced into mobile computing also bring the flexibility to address the limitations of the traditional computing approach.

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**Plenary Address**

**Tuesday, March 19, 2013, 0830 – 1030 Auditorium Dauphine**

Opening Address – Awards – Keynote Speakers

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**First keynote address**

**Smart systems for internet of things**

Benedetto Vigna - Executive VP of STMicroelectronics, IT

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**Second keynote address**

**Creating a sustainable information and communication infrastructure**

Massoud Pedram - Professor at University of Southern California, US

Modern society's dependence on information and communication infrastructure (ICI) is so deeply entrenched that it should be treated on par with other critical lifelines of our existence, such as water and electricity. As is the case with any true lifeline, ICI must be reliable, affordable, and sustainable. Meeting these requirements (especially sustainability) is a continued critical challenge, which will be the focus of my talk. More precisely, I will provide an overview of information and communication technology trends in light of various societal and environmental mandates followed by a review of technologies, systems, and hardware/software solutions required to create a sustainable ICI.

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**Third keynote address**

**Energy efficient computing**

John Goodacre, ARM, UK

Since the first mobile computer, power efficiency was a key measure for success. As the need for performance ever increases, the energy cost of performance has metric well beyond just the life of the battery in mobile. Energy efficiency is now the driver in most consumer products, the compute density of a server, and has become the primary limit in the delivery of high performance. During this talk we will consider the various power related limitations of compute while discovering how the techniques and new capabilities introduced into mobile computing also bring the flexibility to address the limitations of the traditional computing approach.
**High-Performance Low-Power Computing**

**HOT TOPIC - System Approaches to Energy-Efficiency**

*Room - Oisans 0830-1000*

**Organiser:**
Ahmed Jerraya - CEA-LETI-MINATEC, FR

At system level, energy consumption optimisation may be the most rewarding. Different approaches may be applied to improve energy efficiency. This Hot-Topic Session explores both system architecture and applications to reach better energy efficiency.

**EMBEDDED TUTORIAL - HW-SW Architecture Approaches to Energy-Efficiency**

*Room - Oisans 1100 - 1230*

**Organiser:**
Ahmed Jerraya - CEA-LETI-MINATEC, FR

Traditionally HW-SW interfaces are defined twice using two different models: one representing HW from a SW point of view, and one representing SW from a HW point of view. These separate views create a discontinuity in the design process and inevitably induces non-optimised designs from an energy-efficiency point of view. This embedded tutorial presents a HW view, a SW view, and an integrated HW-SW view to study the different approaches to energy efficiency.

**Special Day Keynote**

*Room - Oisans 1330 - 1400*

**ENERGY-EFFICIENT COMPUTING**

John Goodacre - ARM

Since the first mobile computer, power efficiency was a key measure for success. As the need for performance ever increases, the energy cost of performance has metric well beyond just the life of the battery in mobile. Energy efficiency is now the driver in most consumer products, the compute density of a server, and has become the primary limit of high performance. During this talk we will consider the various power related limitations of compute while discovering how the techniques and new capabilities introduced into mobile computing also bring the flexibility to address the limitations of the traditional computing approach.

**HOT TOPIC - Many-Core SoC Approaches to Energy-Efficiency**

*Room - Oisans 1430-1600*

**Organiser:**
Ahmed Jerraya, CEA-LETI-MINATEC, FR

The evolution of the semiconductor industry is allowing intensive computing on a single chip through heterogeneous and homogenous architectures. This increase in compute density on a single chip is both a threat and an opportunity for energy-efficiency. This Hot-Topic Session presents different many-core SoC approaches to improve energy-efficiency.

**HOT TOPIC - Fabrication Technology Approaches to Energy-Efficiency**

*Room - Oisans 1700-1830*

**Organiser:**
Ahmed Jerraya, CEA-LETI-MINATEC, FR

SoC designs integrate an increasing number of heterogeneous programmable units (CPU, GPU, DSP, sub-systems), sophisticated interconnect, innovative memory architecture, and are using energy-efficient libraries that target advanced fabrication process technologies. This Hot-Topic Session presents the key challenges for applying the most advanced fabrication technologies, 3D0I with circuit and architecture technologies to master energy-efficiency.

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**Friday Workshops**

**0730**

**WORKSHOP REGISTRATION & WELCOME REFRESHMENTS**

**BREAKS**

Please see individual workshop programmes for lunch and break times.

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**0830 TO 1700**

**Room - Neige 2**

Room - Staudach

Room - Oisans

Room - Chateau

Room - Eiger

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**Thursday 21 March**

**Special Day - Electronic Technologies for Smart Cities**

**Room - Oisans 08:30 – 10:00**

**Organiser:**
Luca Benini, Università di Bologna, IT

This session will provide a top-down view of energy management and optimization in Smart Environments, with emphasis on Buildings and grid-level integration. The first paper will focus on the design and computer-aided optimization of regional policies for generation, storage and distribution of sustainable energy. The second paper will give a holistic view of grids and building as cyber-physical systems and propose automatic approaches for managing them. Finally, the third paper will look at design challenges for the distributed smart energy metering infrastructure, with the ultimate goal of reaching self-sustainability through energy harvesting.

**09.1**

**HOT TOPIC: Smart Grid and Buildings**

**Room - Oisans 1100 - 1230**

**Organiser:**
Daniele De Venuto, Politecnico di Bari, IT

Alberto Sangiovanni Vincentelli, University of California, Berkeley, US

The Smart Health session is about fundamental technical and scientific advances that may change radically the way Healthcare is conceived today. Longer life expectation, aging, overweight and pollution are among factors that pose severe challenges to healthcare and its sustainability. Wireless devices, brain-machine interfaces, and cognitive process models may provide potential solutions to a vast array of problems involving clinical and human aspects, as well as economics and social issues. The presenters will introduce and discuss some aspects of devices and technologies that are essential in defining new approaches to healthcare and human well-being.

**10.1**

**HOT TOPIC: Smart Data Centers Design and Optimization**

**Room - Oisans 1100-1230**

**Organiser:**
David Atienza, EPFL, CH

This special session presents an overview of some of the hottest research topics towards the conception of future smart and energy-efficient datacenters. The first presentation explores the limits in the conception of highly dense datacenter infrastructures under current and future energy constraints. The second presentation presents smart energy-aware allocation techniques in virtualized datacenters to maximize the use of free cooling. The third presentation explores the limits of energy-efficient servers and resources utilization in next-generation computing systems for datacenters.

**11.0**

**Smart Cities and Communities at the Regional, National and European Levels**

**Room - Oisans 1330 - 1400**

**Francesco Profumo,**
Italian Minister of Education, University and Research

**Genevieve Floraso,**
French Minister for Higher Education and Research

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Friday Workshops

**0830 TO 1700**

**Room - Berlino 2**

Room - Les Bains

Room - Belle-Etoile

Room - Meije 3

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**0830 TO 1700**

**Room - Da Vinci**

**Room - Le Ros**

**Room - Bosco**

**Room - Meije 3**

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**12.1**

**HOT TOPIC: Internet of Energy – Connecting Smart Mobility in the Cloud**

**Room - Oisans 1600-1730**

**Organiser:**
Ovidiu Vermesan, SINTEF, NO

The Internet of Energy (IoE) provides an innovative concept for power distribution, energy storage, grid monitoring and communication. It will allow units of energy to be transferred when and where it is needed. Power consumption monitoring will be performed on all levels, from local individual devices up to national and international level. In this context the new smart electric mobility vehicles will be integrated in the Internet of Energy, creating new mobile ecosystems based on trust, security and convenience to mobile/contactless services and transportation applications will ensure security, mobility and convenience to consumer-centric transactions and services. This special session/workshop will provide different views on the smart mobility concepts and future electric mobility trends by addressing the interaction with the smart city environments in creating an intelligent energy network platform for sustainable transportation systems.
Four of the leading European micro- and nanoelectronics regions are joining their research, development and production expertise to form the transnational, research-driven cluster “Silicon Europe – The Leaders for Energy Efficient ICT Electronics”. The cluster partners from Germany, Belgium, France and the Netherlands are linked by a common goal. They aim to secure and expand Europe’s position as the world’s leading center for energy efficient micro- and nanoelectronics and information and communications technology (ICT). In order to reach this goal, Silicon Saxony (Dresden/Germany), DSP Valley (Belgium), Minalogic (Grenoble/France) and High Tech NL (Eindhoven/Netherlands) are cooperating in research, development and business expertise. Together they represent about 800 research institutes and companies, which account for more than 150,000 jobs; among the companies are global market leaders such as Philips, NXP, Globalfoundries, Infineon, STMicroelectronics, Schneider Electric und Thales. This makes Silicon Europe one of the largest technology clusters of the world.

8.8 HOT TOPIC: Countering Counterfeit Attacks on Micro-Electronics

Organiser: Erik Jan Marinissen - IMEC, BE
Ingrid Verbauwhede - KU Leuven, BE
Chair: Steven Jeter - Infineon Technologies, DE
Co-Chair: Ingrid Verbauwhede - KU Leuven, BE
Counterfeited ICs are an increasing problem. In 2011, a record high of 1,363 counterfeited-part incidents were reported worldwide, representing a $168B risk. Counterfeited incidents include the relatively straightforward extra production at an outsourced manufacturing site for sales through alternative channels, but also the technically more advanced Trojan Horse “sniffer” ICs hidden in a 3D die stack of a telecom product. What can semiconductor suppliers do in technology, design, and test to assure that their customers get to use only genuine components in their systems?

10.8 PANEL: Will 3D-IC Remain a Technology of the Future? Even in the Future?

Organiser: Marco Casale-Rossi - Synopsys, US
Chair: Giovanni De Micheli - EPFL, CH
Co-Chair: Marco Casale-Rossi - Synopsys, US
If asked “who needs faster planes?” the vast majority of the 2.75 billion airline passengers (source: IATA 2011) would say that they do need faster planes, and that they need them right now. Still, the commercial aircrafts cruising speed has remained the same – 800 km/hour – over the last 50+ years, and after the sad end of the Concorde project, neither Airbus nor Boeing are seriously working on the topic. Along the same lines, when asked “who needs 3D-IC?” most IC designers say that they desperately need 3D-IC to keep advancing electronic products performance, whilst addressing the needs of higher bandwidth, lower cost, heterogeneous integration, and power constraints. Still, 3D-IC continues to be the technology of the future. What are the road blocks towards 3D-IC adoption? Is it process technology, foundry or GDSI commercial offering, or EDI, or the business economics that is holding 3D-IC on the ground? In the introductory presentation of this panel session, LETI Patrick Leduc will illustrate the state-of-the-art of commercial, mainstream 3D-IC. EPFL Professor Giovanni de Micheli will moderate an industry and research panel, to understand what are the key factors preventing 3D-IC from becoming the technology of today.

11.8 EMBEDDED TUTORIAL: Advances in Asynchronous Logic: from Principles to GALS & NoC, Recent Industry Applications, and Commercial CAD Tools

Organiser: Pascal Vivet - CEA-LETI, FR
Chair: Robin Wilson - STMicroelectronics, FR
Co-Chair: Beigl Edith - CEA-LETI, FR
The growing variability and complexity of advanced CMOS technologies makes the physical design of clocked logic in large Systems-on-Chip more and more challenging. Asynchronous logic has been studied for many years and become an attractive solution for a broad range of applications, from massively parallel multi-media systems to systems with ultra-low power & low-noise constraints, like cryptography, energy autonomous systems, and sensor networks. This tutorial is to give a comprehensive and recent overview of asynchronous logic. The tutorial will cover the basic principles and advantages of asynchronous logic, some insights on new research challenges, and will present the GALS scheme as an intermediate design style with recent results in asynchronous Network-on-Chip for future Many Core architectures. Regarding industrial acceptance, recent asynchronous logic applications within the microelectronics industry will be presented, with a main focus on the commercial CAD tools available today.
INTERACTIVE PRESENTATIONS

Interactive presentations allow presenters to interactively discuss novel ideas and work in progress that may require additional research work and discussion, with other researchers working in the same area. Interested attendees can walk around freely and talk to any author they want in a vivid face-to-face format. The author may illustrate his work with a slide show on a laptop computer, a demonstration, etc. IP presentations will also be accompanied by a poster. Each IP will additionally be introduced in a relevant regular session prior to the IP Session in a one-minute presentation.

To give an overview, there will be one central projection displaying a list of all the presentations going on at the same time in the IP area.

Interactive Sessions will be held in the Exhibition Hall in 30-minute time slots during exhibition and coffee breaks.
Design Automation Conference

JUNE 2-6, 2013
AUSTIN, TX

Where IC Design and the EDA ecosystem learns, networks, and conducts business.

DAC is the largest conference focused on electronic design, IP and embedded systems and software (ESS).

DAC Delivers:
- An exciting technical program on Electronic Design Automation and Embedded Systems & Software (ESS)
- Daily Keynotes, presented by Top Industry Executives
- Management Day: The Edge of Business and Technology
- Designer/User Track presentations by and for users
  Sponsored by ANSYS, Apache
- Colocated Conferences, Tutorials and Workshops
- Over 175+ Exhibitors including NEW Innovation Square & The ARM Connected Community® (CC) Pavilion

DAC.COM

BEST REASONS TO ATTEND!

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The Design Automation Conference (DAC) is the leading technical conference and tradeshow on electronic design, design automation, embedded systems and software. It is where IC Design and the EDA ecosystem features over 300 presentations consisting of technical sessions, panels, exciting keynotes, covering the latest in design methodologies, embedded software and EDA tool developments. The exhibition offers booths and suites from over 175 of the leading EDA, providers. 50th DAC, June 2 – 6, 2013, Austin Convention Center. www.dac.com.

We are a small company that provides an all-in-one development environment for application processors and ASIC design services. Our Codasip® Framework enables designers to create the most effective Application-Specific Instruction-set Processors (ASIPs) for both the target applications, and the application domain. Our customized Codasip® Framework outperforms related Synopsys and Cadence development tools in many aspects. Through the use of Codasip® Framework you will shorten development time substantially and you will deliver higher performance ASIPs. Codasip® Framework incorporates the innovative feature of the automated generation of the OVM based functional verification. As a result of this unique functionality, designers utilize fluent flow from the processor specification to the validation of the generated C/C++ compiler when compared to the generated synthesizable RTL. The time savings are achieved through the automation of tasks that would otherwise be done manually, including the fully automatic generation of the programming and simulation toolchain, and the generation of the synthesizable RTL and support of functional verification.

PRODUCT FINDER
ASIC and SOC Design: Design Entry
Power & Optimisation
Verification
System-Level Design: Behavioural Modelling & Analysis Acceleration & Emulation Hardware/Software Co-Design
Services: Design Consultancy Prototyping Training
Embedded Software Development: Compilers Debuggers Software/Modelling
Hardware: FPGA & Reconfigurable Platforms
Semiconductor IP: CPUs & Controllers On-Chip Bus Interconnect On-Chip Debug
Processor Platforms
Application-Specific IP: Digital Signal Processing Multimedia Graphics

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E-Mail: info@codasip.com
Website: www.codasip.com

We are excited to announce Release 6.0 of Blue Pearl Software Suite which includes comprehensive RTL analysis, clock-domain crossing (CDC) checks, and automatic SDC generation for SoC designs. Blue Pearl Software Suite is easy to use for any level of ASIC/FPGA designers.

Our Software Suite which runs on Windows and Linux, offers multi-language (Verilog, SystemVerilog and VHDL) support, and supports major synthesis flows. Designers can mix and match hardware languages in the same design with language checking that matches downstream tools. Its visualization and validation technology gives immediate feedback for validating its automatically generated timing constraints.

PRODUCT FINDER
ASIC and SOC Design: Design Entry
Behavioural Modelling & Simulation Synthesis Power & Optimisation
Physical Analysis (Timing, Thermal, Signal) Verification
Analog and Mixed-Signal Design MEMS Design
RF Design
System-Level Design: Behavioural Modelling & Analysis Physical Analysis Acceleration & Emulation Hardware/Software Co-Design
Test: Design for Test Design for Manufacture and Yield Test Automation (ATPG, BIST) Silicon Validation Mixed-Signal Test
Services: Prototyping Foundry & Manufacturing Training
Embedded Software Development: Compilers Real Time Operating Systems Software/Modelling
Shared Service Platform for Micro-electronic focuses on SMEs and startups seeking access to ED A and embedded software design tools for usage patterns that do not justify the purchase or lease of costly annual licenses. From the facilities and infrastructures allowing companies to use the ED A tools and computing infrastructure already installed and preconfigured. The time for a company to be fully operational is therefore considerably shortened. In addition, Minalogic ensures that value provided by Cim Alpes and how it to design micro-nanoelectronics systems. Moreover, the access to design kits can be Cim Alpes offers users special rates that include an annual membership that depends on the size of the company and variable rental cost based on their usage time (pay per use model).

The primary objective of the COMPLEX (CODesign and power Management in Platform-based design space EXPloration) European Integrated Project has been to develop an innovative, highly efficient and productive design methodology and a holistic framework for iteratively exploring the design space of embedded HW/SW systems. COMPLEX focussed on early, fast yet accurate platform-based design space exploration at the system level.

The COMPLEX consortium has developed a new design environment for platform-based design-space exploration offering developers of next-generation mobile embedded systems a highly efficient design methodology and tool chain. The integrated environment allows iterative exploration and refinement of advanced applications to meet market requirements. The design technology in particular enables fast simulation and assessment of the platform at Electronic System Level (ESL) with up to bus-cycle accuracy at the earliest instant in the design cycle.

Partners: OFFIS (DE), STMicroelectronics (IT), STMicroelectronics (CN), Thales Communications (FR), GMV (ES), Synopsys (BE), EDALab (IT), Magillem Design Services (FR), Politecnico di Milano (IT), Universidad de Cantabria (ES), Politecnico di Torino (IT), IMEC (BE), ECSI (FR)

PRODUCT FINDER
ASIC and SOC Design:
Design Entry
Behavioural Modelling & Simulation
Power & Optimisation
System-Level Design:
Behavioural Modelling & Analysis
Hardware/Software Co-Design

Concept Engineering GmbH

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Tel: +49 761 470940
Fax: +49 761 4709429
E-Mail: info@concept.de
Website: www.concept.de

Concept Engineering develops and markets innovative visualization and debugging technology for commercial EDA vendors, in-house CAD tool developers, FPGA and IC designers. Nview WidgetsTM – a family of schematic generation and visualization engines (Tcl/TK, MFC, Qt, Java, Perl/Tk, wxWidgets) that can be easily integrated into EDA tools. RTLVisionTM PRO – a graphical debugger for SystemsVerilog, Verilog and VHDL based designs. GateVision® PRO – a customizable debugger for Verilog, LEF/DEF and
EDIF based designs.
SpiceVision® PRO – a customizable debugger for SPICE based designs.
S@VisionTM PRO – a customizable mixed-mode debugger (SPICE and Verilog).
StarVisionTM PRO - a customizable mixed-signal and mixed-language debugger.

**PRODUCT FINDER**

**ASIC and SOC Design:**
- Verification
- Analogue and Mixed-Signal Design
- Test:
  - Mixed-Signal Test

**CST - Computer Simulation Technology AG**

**Contact:** Jerome Mollet
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**Fax:** +49 6151 7303 100
**E-Mail:** info@cst.com
**Website:** www.cst.com

CST develops and markets high performance software for the simulation of electromagnetic fields in all frequency bands. Its products allow you to characterize, design and optimize electromagnetic devices all before going into the lab or measurement chamber. This can help save substantial costs especially for new or cutting edge products, and also reduces design risk and improves overall performance and profitability. Its success is based on the implementation of leading edge technology in a user-friendly interface. Furthermore, CST’s “complete technology” complements its market and technology leading time domain solver (CST MICROWAVE/STUDIO®), thus offering unparalleled speed, accuracy and versatility for all applications. CST’s customers operate in industries as diverse as Telecommunications, Defense, Automotive, Electronics, and Medical Equipment, and include market leaders such as IBM, Intel, Mitsubishi, Samsung, and Siemens. CST markets its products worldwide through a network of distribution and support centers which also provide comprehensive customer support and training.


**System-Level Design:**
- Behavioural Modelling & Analysis
- Physical Analysis
- Package Design
- PCB & MCM Design

**Test:**
- Design for Test

**Embedded Software Development:**
- Software/Modelling

**DeFacTo Technologies**

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**Website:** www.defactotech.com

DeFacTo Technologies provides innovative and non-intrusive EDA solutions to help achieving “Design & DFT” closure at RTL by delivering a high quality suite of tools which cover IP Integration, Design Verification & DFT Signoff needs.

**PRODUCT FINDER**

**ASIC and SOC Design:**
- Design Entry
- Verification

**Test:**
- Design for Test
- Test Automation (ATPG, BIST)
- Boundary Scan

**Design and Reuse**

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**E-Mail:** gabriele.saucier@design-reuse.com
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**DOCEA Power**

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**Website:** www.doceapower.com

DOCEA Power develops and markets dedicated system-level tools for modeling and optimizing power/thermal behavior of whole electronics systems. DOCEA’s Aceplorer software offers a framework to capture all power related data in a single environment and integrates a consistent methodology for modeling and simulating the power behavior of electronics systems, from SoCs, to systems-in-package and complete boards. The “separation of concerns” approach makes Aceplorer’s standalone power models usable across teams and project stages from system level early measurements, to power budget tracking and to silicon validation.

The Aceplorer innovative platform is the solution for early power estimation, architecture and power management strategies exploration, use case profiling, package selection and other technology choices that are impacted by power consumption and thermal distribution. Dealing with power and/or thermal issues with Aceplorer Power solutions at system level is fast, secure and efficient. DOCEA technology has been adopted by world’s largest semiconductor companies as well as major system integrators in the mobile communications industry.

**PRODUCT FINDER**

**ASIC and SOC Design:**
- Power & Optimisation

**System-Level Design:**
- Behavioural Modelling & Analysis

**Test:**
- System Test

**Services:**
- Training

**Embedded Software Development:**
- Software/Modelling

**Dolphin Integration**

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Dolphin Integration (www.dolphin-ip.com) is a developer and marketer of virtual components of Intellectual Property partaking in the design of multi-domain Integrated Circuits with a focus on Systems-on-Chip and MEMS with micromechanical structures. The range of products includes:

* a handful of microprocessors in synthesizable logic VHDL or Verilog around the Flip8051,
* the library of standard cells with generators of embedded RAMs and ROMs, down to 65 nm, patented for high density and low power-consumption, with the unique advantage to enable Back-Tracking Free Placement and Routing.
* as well as Virtual Components for high resolution for Voice and Audio applications such as Portable Multimedia Players, and Sensors for high resolution measurements.

Their secret weapon is multi-level simulator SMASH All-in-1, the best VHDL-AMS solution with its powerful add-ons for Multi-Domain Modeling.

The company has been active since 1985 and has received the ISO-9001: 2000 certification.

PRODUCT FINDER
ASIC and SOC Design:
- Design Entry
- Behavioural Modelling & Simulation
- Synthesis
- Power & Optimisation
- Physical Analysis (Timing, Thermal, Signal)
- Verification
- Analogue and Mixed-Signal Design
- MEMS Design
- RF Design
System-Level Design:
- Behavioural Modelling & Analysis
- Hardware/Software Co-Design
Services:
- Design Consultancy
- Prototyping
Semiconductor IP:
- Analogue & Mixed Signal IP
- Configurable Logic IP
- CPUs & Controllers
- Memory IP
- Physical Libraries
- Processor Platforms
- Synthesizable Libraries
Application-Specific IP:
- Analogue & Mixed Signal IP
- Telecommunication
- Wireless Communication

For over 10 years EDA Solutions have provided cost effective and highly productive IC Design software and manufacturing services to European industry. Visit us on Stand 7 to find out more about the digital synthesis tools from Incentia, the analog/mixed signal design, layout and verification tools from Tanner EDA and the MPW and low volume production services from MOSIS.

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Fax: +33.(0)4.76.67.36.99
E-Mail: billon@edxact.com
Website: www.edxact.com

EDXACT focuses on design tools aimed at physical design and verification of Integrated Circuits, with a specialization on questions related to netlist parasitics and their impact on simulation time, signal integrity, delay, crosstalk and other. EDXACT is best known for netlist reduction technology JIVARO, offering additional dedicated analysis tools BELLEDONNE and VISO. http://wwwedxact.com

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"SoC Memory Management made easy"

PRODUCT FINDER
Semiconductor IP:
- Configurable Logic IP
- CPUs & Controllers
- Embedded FPGA
- Embedded Software IP
- Memory IP
- On-Chip Bus Interconnect
- Processor Platforms
Application-Specific IP:
- Data Communication

For over 10 years EDA Solutions have provided cost effective and highly productive IC Design software and manufacturing services to European industry. Visit us on Stand 7 to find out more about the digital synthesis tools from Incentia, the analog/mixed signal design, layout and verification tools from Tanner EDA and the MPW and low volume production services from MOSIS.

The EUROPRACTICE IC service offers low cost and easy access to ASIC prototype and small volume fabrication. The service is offered by IMEC (B) and FhG/IIS (D). Low cost prototyping is achieved by offering fabrication through regularly scheduled MPW (Multi Project Wafer) runs whereby many designs from different customers are merged onto the same fabrication run. These runs are fabricated in industrial CMOS, BiCMOS and SiGe processes from 0.7µ to 40nm at well-known foundries (ONSemiconductor, austriamicrosystems, IHP, LFoundry, TSMC, UMC). A total integrated design and manufacturing flow is offered including cell library and design kit access and support, deep submicron netlist-to-layout, ASIC prototyping on MPW or dedicated single project prototype runs, volume fabrication, qualification, assembly and test. Volume fabrication starts with wafer batches as low as 12 wafers but can go up to more than 5000 wafers per year per ASIC. The EUROPRACTICE IC service offers low cost and easy access to ASIC prototype and small volume fabrication. The service is offered by IMEC (B) and FhG/IIS (D). Low cost prototyping is achieved by offering fabrication through regularly scheduled MPW (Multi Project Wafer) runs whereby many designs from different customers are merged onto the same fabrication run. These runs are fabricated in industrial CMOS, BiCMOS and SiGe processes from 0.7µ to 40nm at well-known foundries (ONSemiconductor, austriamicrosystems, IHP, LFoundry, TSMC, UMC). A total integrated design and manufacturing flow is offered including cell library and design kit access and support, deep submicron netlist-to-layout, ASIC prototyping on MPW or dedicated single project prototype runs, volume fabrication, qualification, assembly and test. Volume fabrication starts with wafer batches as low as 12 wafers but can go up to more than 5000 wafers per year per ASIC.

AEPi is the economic development agency for Grenoble-Isere/France. The Grenoble area, smart valley in southeastern France, is Europe’s top center in micro-nanotechnologies and derived applications, and home of the program Nano2012, representing over 2.3 billion investment on the Croises STMicroelectronics site. Working closely with Minatec-CEA-Leti as well as the industrial cluster Minalogic, AEPi provides complimentary information and services to companies exploring business opportunities.

Grenoble-Isère/AEPI
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A EPI is also a member of the local board of the Semi Europe Grenoble office, located on the Minatec Campus, and is an active supporter of the European cooperation between Silicon Saxony and Grenoble microelectronics clusters.

The HiPEAC network of excellence (i) steers to systems; (ii) improves the quality of such research, (iii) and creates a visible and integrated pan-European community in computing systems. The membership program aims at growing the network. It creates a vibrant industrial membership and reaches out to companies and academics in the new member states and beyond. The mobility program brings the partners and the members closer together by funding one-to-three month internship exchanges, collaboration grants, mini-sabbaticals and by organizing networking events. The research coordination program aims at coordinating the joint research between the HiPEAC members. A tangible result of the research coordination is the network such as an annual conference, the summer school, the HiPEAC website, a quarterly newsletter and the award program.

The main goal of the project is to define innovative methodologies for system-level design, able to guide designers and researchers to the optimal composition of embedded MPSoC architecture, according to the requirements and the features of a given target application field. The proposed methodologies will extend the classic concept of design space exploration to:

- Improve design predictability, bridging the so called “implementation gap”, i.e. the gap between the results that can be predicted during the system-level design phase and those eventually obtained after the on-silicon implementation.
- Consider, in addition to traditional metrics (such as cost, performance and power consumption), continued availability of service, taking into account fault resilience as one of the optimization factors to be satisfied.
- Support adaptive runtime management of the architecture, considering, while tailoring the architecture, new metrics posed by novel dynamic strategies and advanced support for communication issues that will be defined.

Incentia Design Systems, Inc. is a leading provider of advanced Timing and Signal Integrity Analysis, Design Closure, and Logic Synthesis software for multi-million-gate nanometre designs. Incentia patented technologies provide the fastest Static Timing Analysis (STA) tool in the market today.

Incentia’s products are in use at leading semiconductor, fabless IC design, systems, and design service companies worldwide and have produced numerous customer tape-outs, including those using advanced 40nm technologies and designs over 50 million gates. Incentia are represented in Europe by EDA Solutions, who will be happy to explain more to you about our services, and answer any questions you may have. Why not come to Stand 7 or visit the EDA Solutions website www.eda-solutions.com for more details.

Minalogic brings together the Rhône- Alpes region’s leading innovators in the field of smart miniaturized systems. By leveraging the Grenoble area’s synergies between research, higher education, and industry, we have achieved a global leadership position in smart embedded systems. Our cluster actively facilitates networking among innovators, manufacturers, and investors to get new technologies to market quickly. The technologies developed at the cluster are applicable to all business sectors, including more traditional industries. The role of Minalogic is to respond to the business community’s need to identify new value-added products in fields that include health care, the environment, mobility, the media, and the textile industry.

Incentia's products are in use at leading semiconductor, fabless IC design, systems, and design service companies worldwide and have produced numerous customer tape-outs, including those using advanced 40nm technologies and designs over 50 million gates. Incentia are represented in Europe by EDA Solutions, who will be happy to explain more to you about our services, and answer any questions you may have. Why not come to Stand 7 or visit the EDA Solutions website www.eda-solutions.com for more details.

MOSIS is a low-cost prototyping and small-volume production service for VLSI circuit development. Since 1981, MOSIS has fabricated more than 50,000 circuit designs for commercial firms, government agencies, and research and educational institutions around the world. Processes offered include SOS, SOI, CMOS and SiGe BiCMOS, in
geometries from 0.7μm to 32nm, from the foundries IBM, TSMC, ON Semiconductor, austriamicrosystems, Globalfoundries, and Peregrine. MOSIS are represented in Europe by more to you about our services, and answer any questions you may have. Why not come to Stand 7 or visit the EDA Solutions website www.eda-solutions.com for more details.

MunEDA provides leading EDA software technology for analysis, modelling and optimization of yield and performance of analog, mixed-signal and digital designs. MunEDA’s products and solutions enable customers to reduce the design times of their circuits and to maximize robustness, reliability and yield. MunEDA’s solutions are in industrial use by leading semiconductor companies in the areas of communications, computer, memories, automotive, and consumer electronics.

The research involves more than 700 researchers and 31 Swiss research institutions, yielding about 575 publications and 1000 presentations in conferences and workshops, as well as several presentations in the media. 30 industrial partners are involved in the projects and a total of 15 patent applications have been filed so far.

Electronic design automation (EDA) supplier OneSpin Solutions of Munich, Germany, was founded in 2005 as a spin-off from Infineon Technologies AG. It leverages more than 300 engineer-years of formal verification technology development and application service experience to enable design teams to avoid costly redesigns and respins, while dramatically cutting their verification effort and costs and time-to-market pressures. Market-leading telecommunication, automotive, consumer electronics, and embedded systems companies rely on OneSpin to reduce their verification effort and achieve the industry’s highest possible verification quality.

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The PHARAON project is a European collaborative initiative between universities, research labs and industrials. It is sponsored by the European Commission that supports part of the costs and assists partners in the project management. The main objective of PHARAON is to improve competitiveness of the European embedded electronic industry, especially with respect to reducing power consumption and improving performance, by providing new paradigms for multicore architectures programming, monitoring and control, as well as new dynamic power adaptation strategies, algorithms and interfacing standards. Raising the expertise of European industry in system architecture, software development and power management is crucial to ease the transition to multicore platforms. It will enlarge the range of applicability of a hardware platform and plays in favour of re-use, cost and time-to-market reduction, which have become crucial requirements in a worldwide competition. Partners: Thales Communications & Security, Politecnico di Torino, IMEC, University of Cantabria, ENS, Teelsey, Vector Fabrics

Interactive Presentations will be held in the Exhibition Hall in 30-minute time slots during exhibition and coffee breaks.
Presto Engineering has been created in 2006 (San Jose, California) and has now global hubs in USA, Israel and Europe (Grenoble and Caen). Presto Engineering is a global engineering services provider for the overall complex IC’s. Our focus is in RF and high-customers, we deliver Test Engineering, Characterization, Qualification and Failure Analysis. We also support Test Production, Assembly, Yield Management and Turn-Key Solution with wafer fab foundries. Presto Engineering provides also Consulting Services including Audits (tier party Audits, Manufacturing lines,...), Consulting and Assistance, Training (FA techniques,...), Different platforms are available in Presto Engineering to perform Test Engineering and Characterization (V93K Verigy, LTX X-Series MX, µFlex Teradyne,....). We handle all the tests needed for a qualification (HTOL, HAST, TMCL,...). Our team supports also the hardware development for these Test and qualification fields. We have all the techniques needed for FA in order to address the most advanced technologies. Presto Engineering is ISO9001:2008 certified and COFRA ISO17025:2005 accredited.

Politecnico di Torino, with over 27,000 students, is the second largest technical university in Italy. The workforce dedicated to research and teaching includes around 900 Professors, 700 PhD Students and 300 Research Assistants, covering all major areas of the engineering and architecture disciplines.

Serma Technologies is an FA Laboratory and a Test house Company (170 people) located in Paris, Bordeaux and Grenoble and part of the Serma Group (670 people, 80 Million Euros Turnover). The company offers services such as: - Test Program Development including DfT - Test Production - Supply Chain Management - Environmental & ESD Qualification according to standards (JEDEC, MIL, AEC100). - Failure Analysis (Wafer, Die, Component, System).

PRODUCT FINDER
ASIC and SOC Design:
Physical Analysis (Timing, Thermal, Signal)
System-Level Design:
Physical Analysis
Hardware/Software Co-Design
Test:
Design for Test
Design for Manufacture and Yield
Logic Analysis
Test Automation (ATPG, BIST)
Boundary Scan
Silicon Validation
Mixed-Signal Test
System Test
Services:
Training
Application-Specific IP:
Security

Solvtec is an EDA start-up that responds to the biggest bottleneck in the design of digital integrated circuits: the localization and fixing of bugs (debugging tool). Solvtec's next generation RTL debugging tool DebugIt reduces the time-to-market of chip designs by adding automated analysis for bug localization and bug fixing to basic debugging functionalities. DebugIt automatically pinpoints bug locations in HDL code, classifies bug locations, checks bug responsibility of third party IP, provides explanations and hints to fix and assigns bugs to the respective chip design engineers.

Tanner EDA provides a complete line of software solutions that catalyze innovation for the design, layout and verification of analog and mixed-signal (A/M) integrated circuits (ICs). Customers are creating breakthrough applications in areas such as power management, displays and imaging, automotive, consumer electronics, life sciences, and RF devices. Tanner are represented in Europe by EDA Solutions, who
will be happy to explain more to you about our services, and answer any questions you may have. Why not come to Stand 7 or visit the EDA Solutions website www.eda-solutions.com for more details.

### PRODUCT FINDER

**ASIC and SOC Design:**
- Design Entry
- Behavioural Modelling & Simulation
- Verification
- Analogue and Mixed-Signal Design
- MEMS Design
- RF Design
- Test:
  - Silicon Validation
  - Mixed-Signal Test

### Target Compiler Technologies

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Target Compiler Technologies is the leading provider of retargetable software tools for the design, programming and verification of application-specific processor cores (ASIPs). ASIPs are key building blocks of single- and multi-core systems-on-chip (SoCs) that power today’s electronic systems. IP Designer, Target’s flagship product, enables the design of ASIPs with performance and energy characteristics close to hardwired datapaths. Yet these ASIPs provide software programmability, thus permitting changes in specifications and extending the revenue lifetime of SoCs. IP Designer supports ASIC architectural exploration, and generates a complete C compiler based software development kit as well as a low-power hardware implementation for each ASIC. The tools have been used by customers around the globe to design SoCs for 2G/3G/4G handsets, cordless and VoIP phones, audio/video/image processing, infotainment and security for cars, DSL modems, DSL access multiplexers, wireless LAN, hearing instruments, and personal health-care systems. Target is also introducing MP Designer, a new tool for multicore parallelisation and design in an SoC context. URL: www.retarget.com

### The IET

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The IET is europe’s largest professional body for engineers and technologists, we offer a wide range of products, services and professional qualifications to keep you ahead of the game. With 150,000 members based in 127 countries networking is key to their and your success - find out how to join and be part of the Knowledge Network by visiting us at our stand or visit www.theiet.org

### Xyalis

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XYALIS introduces its new highly parallel CMP metal fill engine at the Date Conference, GStyle. The new GStyle release has been successfully used on a multi-billion transistor processor design using TSMC 28nm process, in a few hours, allowing metal fill to be run as part as the design flow. XYALIS will also present its proven integrated Mask Data Preparation solution automating frame generation, multichip assembly, mask set creation, and mask order form management, which shortens time to manufacturing, Increases yield, and removes errors during mask and wafer production.

### University Booth

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Fax: +49 (511) 762-19695 (Andreas Vörg)  
E-Mail: university-booth@date-conference.com  
Website: date-conference.com/group/exhibition/u-booth

The University Booth is part of the DATE program and is sponsored by the DATE Sponsor Society. The University Booth will be organized for EDA software and hardware demonstrations. Universities and public research institutes are presenting innovative hardware and software demonstrations. All demonstrations will take place during the exhibition within a dedicated time slot. The University Booth is organized by Laurent Fesquet (TIMA) and Andreas Vörg (edacentrum).

### EDAC Solutions

**Website:** www.eda-solutions.com

Reasonable hardware is a must for any electronics system, but to be truly successful it has to work well with other aspects of the system. EDAC Solutions will be showcasing our range of high quality electronic components.
Scope of the Event
The 17th DATE conference and exhibition is the main European event bringing together designers and design automation users, researchers and vendors, as well as specialists in the hardware and software design, test and manufacturing of electronic circuits and systems. It puts strong emphasis on both ICs/SoCs, reconfigurable hardware and embedded systems, including embedded software.

Structure of the Event
The five-day event consists of a conference with plenary invited papers, regular papers, panels, hot-topic sessions, tutorials, workshops, two special focus days and a track for executives. The scientific conference is complemented by a commercial exhibition showing the state-of-the-art in design and test tools, methodologies, IP and design services, reconfigurable and other hardware platforms, embedded software, and (industrial) design experiences from different application domains, such as automotive, wireless, telecom and multimedia applications. The organization of user group meetings, fringe meetings, a university booth, a PhD forum, vendor presentations and social events offers a wide variety of extra opportunities to meet and exchange information on relevant issues for the design and test community. Special space will also be allocated for EU-funded projects to show their results. More details are given on the DATE website (www.date-conference.com).

Areas of Interest
Within the scope of the conference, the main areas of interest are: embedded systems, design methodologies, CAD languages, algorithms and tools, testing of electronic circuits and systems, embedded software, applications design and industrial design experiences. Topics of interest include, but are not restricted to:

- System Specification and Modeling
  - System Design, Synthesis and Optimization
  - Simulation and Validation
  - Design of Low Power Systems
  - Power Estimation and Optimization
  - Emerging Technologies, Systems and Applications
  - Formal Methods and Verification
  - Network on Chip
  - Architectural and Microarchitectural Design
  - Architectural and High-Level Synthesis
  - Reconfigurable Computing
  - Logic and Technology Dependent Synthesis for Deep-Submicron Circuits
  - Physical Design and Verification
  - Analogue and Mixed-Signal Circuits and Systems
  - Interconnect, EMC, EMD and Packaging Modeling

- Computing Systems
- Communication, Consumer and Multimedia Systems
- Transportation Systems
- Medical and Healthcare Systems
- Energy Generation, Recovery and Management Systems
- Secure, Dependable and Adaptive Systems
- Test for Defects, Variability, and Reliability
- Test Generation, Simulation and Diagnosis
- Test for Mixed-Signal, Analog, RF, MEMS
- Test Access, Design-for-Test, Test Compression, System Test
- On-Line Testing and Fault Tolerance
- Real-time, Networked and Dependable Systems
- Compilers and Code Generation for Embedded Systems; Software-centric System Design Exploration
- Model-based Design and Verification for Embedded Systems
- Embedded Software Architectures and Principles: Software for MPSoC, Multi/many-core and GPU-based Systems

Submission of Papers
All papers have to be submitted electronically by Friday September 13, 2013 via: http://www.date-conference.com/
Papers can be submitted either for standard oral presentation or for interactive presentation.

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