With the increasing SoC complexity and time-to-market pressure, \textit{platform-based design} is becoming a new paradigm for the design and analysis of embedded systems. Among its advantages, this methodology favors design reuse, architecture exploration, and early software development. It allows to raise the abstraction level to ESL (Electronic System Level). In that ESL context, \textit{SystemC TLM} (Transaction-Level Modeling) is perceptibly being adopted, and TLM specifications tend to become \textit{golden reference models}. Their reliability is therefore capital, and guaranteeing their correctness is compelling. \textit{Assertion-based verification} is an efficient way to reach that target.

**Assertion-based Verification and TLM**

In the last decade, \textit{assertion-based verification} (ABV) has widely gained acceptance. Assertions expressed in languages like the IEEE standard PSL [PSL] are used to specify logical and temporal properties that the design under development is to satisfy. This is now a well-established technology at the RT level. Even if various efforts have recently been reported, there is nowadays no simple and effective solution for ABV at the transactional level.

SystemC TLM specifications are algorithmic descriptions in which communications are implemented as \textit{function calls}. Time can be introduced, but there is no \textit{synchronization clock}, and even no notion of cycle-accuracy at the highest abstraction levels. Thus there is a crucial need for ABV solutions that do not rely on discrete time models associated with clocked contexts. Moreover, being able to make use of the \textit{Modeling layer} of PSL is very desirable: this layer enriches PSL by giving the ability to introduce auxiliary variables in the assertions; it is mandatory for expressing most non-trivial properties of TLM models.

**The ISIS tool**

In this demonstration, we present ISIS [FP10a], our prototype tool for the verification of temporal properties during SystemC simulation (for timed or untimed TLM specifications). It also supports auxiliary variables managed through the PSL Modeling layer [FP10b]. We illustrate its capabilities on several examples, among which:

- a platform with a DMA controller. Example properties for this DMA are:
  - \textit{any time the control register of the DMA is programmed, an end-of-transfer notification occurs before the next writing into the control register.}
  - \textit{any time a source address is transferred to the DMA, a read access in the memory eventually occurs and the right address is used.}

- a system with a 4x4 multicast helix packet switch. Example properties are:
  - \textit{every packet sent by a sender X to a receiver Y will eventually be delivered}
  - \textit{two packets sent sequentially on the same input to the same destination will be received in the same order.}

- a Motion-JPEG decoding platform. Example property is: \textit{the data (images) that are written on the RAMDAC are exactly the ones that have been transmitted by the processing unit (reliability of the communication channel).}

**References.**

