HOW TECHNOLOGY R&D LEADERSHIP BRINGS
A COMPETITIVE ADVANTAGE
IN THE FIELDS OF MULTIMEDIA CONVERGENCE
AND POWER APPLICATIONS

Philippe MAGARSHACK
STMicroelectronics
Technology R&D Group VP
Crolles, France
Outline

- Identifying the fundamental post-recovery market changes: uncovering the new driving applications
  - Understanding the crucial benefits of technology leadership
  - An ST case study: ST Leadership in Technology & ST Competitive Advantage
TAM Market trend line
Monthly B Unit and B $ value

Source: WSTS

DATE - March 2011
Maturing Market

Long term CAGR moved from 15% to 7%
But pervasion is not ending
Key Driving - Loosing Applications
2010-2014* Estimates – TAM Variation in M$

(1) Total Industrial sector includes medical, automation and other sub-segments.

* Source: iSuppli, available only until 2014
Market trend by Applications

2010 Semiconductor Market

- Industrial: 39%
- Automotive: 21%
- Consumer: 19%
- Wireless: 7%
- Wired: 6%
- Data Processing: 9%

CAGR 2010 – 2014*

- Industrial: 4.9%
- Automotive: 8.2%
- Consumer: 4.5%
- Wireless: 8.9%
- Wired: 4.9%
- Data Processing: 1.5%

* Source: iSuppli, available only until 2014
## Semi Industry’s Changing Geography

<table>
<thead>
<tr>
<th>Year</th>
<th>1980</th>
<th>1990</th>
<th>2000</th>
<th>2010</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>USA TI</td>
<td>Japan NEC</td>
<td>USA Intel</td>
<td>USA Intel</td>
</tr>
<tr>
<td>1</td>
<td>USA Motorola</td>
<td>Japan Toshiba</td>
<td>Japan Toshiba</td>
<td>USA Samsung</td>
</tr>
<tr>
<td>2</td>
<td>USA Philips</td>
<td>USA Motorola</td>
<td>Japan NEC</td>
<td>USA TI</td>
</tr>
<tr>
<td>3</td>
<td>Japan NEC</td>
<td>Japan Hitachi</td>
<td>Japan Samsung</td>
<td>Japan Renesas</td>
</tr>
<tr>
<td>4</td>
<td>USA National</td>
<td>USA Intel</td>
<td>USA TI</td>
<td>Hynix</td>
</tr>
<tr>
<td>5</td>
<td>Japan Toshiba</td>
<td>Japan Fujitsu</td>
<td>USA ST</td>
<td>USA ST</td>
</tr>
<tr>
<td>6</td>
<td>Japan Hitachi</td>
<td>USA TI</td>
<td>Japan Motorola</td>
<td>Micron</td>
</tr>
<tr>
<td>7</td>
<td>USA Intel</td>
<td>Japan Mitsubishi</td>
<td>Japan Infineon</td>
<td>USA Qualcomm</td>
</tr>
<tr>
<td>8</td>
<td>USA Fairchild</td>
<td>Philips</td>
<td>Japan Hitachi</td>
<td>Japan Elpida</td>
</tr>
<tr>
<td>9</td>
<td>USA Siemens</td>
<td>Matsushita</td>
<td>USA Micron</td>
<td>USA Micron</td>
</tr>
<tr>
<td>10</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Sources: Future Horizons, Gartner, iSuppli
1. Industry is maturing
2. **Industry is consolidating / specializing**
3. Semiconductor market keeps moving East
4. **Leading-edge processes within few actors**
5. **Convergence is accelerating**
6. New software trends reshape the market forces
7. **Home and mobile appliances become nodes of the Web**
8. **R&D is shifting across the value chain**
9. Semiconductors are key enablers of environmental policies
Identifying the fundamental post-recovery market changes:
  uncovering the new driving applications

Understanding the crucial benefits of technology leadership

An ST case study: ST Leadership in Technology & ST Competitive Advantage
DIFFERENT PARADIGM => DIFFERENT NEEDS

**SOC**
MULTI-FUNCTIONAL
Mobile Internet Device
- High-Speed >2GHz
- Low Operation Vdd
- Low Stdby Leakage

**MPU**
MONO-FUNCTIONAL
Computers, Servers
- High-Speed >>2GHz
- High Operation Vdd
- High Stdby Leakage

⇒ different technologies needed
MULTITUDE OF FUNCTIONS => MULTITUDE of TECHNOLOGICAL REQUIREMENTS TO RECONCILE

Extremely High Speed in Burst mode
High Speed Pdyn limited
Static Power VddRet as low as possible
voltage, surface F\text{t}, F_{\text{max}}, \text{ESD}

Density, Process compatibility
RF f_c, f_{\text{max}}, matching, Noise
Area Low V_{\text{dd}} op. V_{\text{min}} as low as possible

High Voltage Operation, data transfer

HIGH VOLTAGE => HIGH SPEED

PROCESS-DESIGN ENABLEMENT-ARCHITECTURE CIRCUIT-PACKAGE

DATE - March 2011
MULTITUDE OF FUNCTIONS => MULTITUDE of TECHNOLOGICAL REQUIREMENTS TO RECONCILE

Digital Library
-15%
New LDMOS
-20%
New ESD
-40%

Courtesy BOSCH AE
## Technology Platform Segmentation

<table>
<thead>
<tr>
<th>High Performance</th>
<th>Computers</th>
</tr>
</thead>
<tbody>
<tr>
<td>“HP”</td>
<td></td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>General Purpose</th>
<th>Computer Peripherals</th>
</tr>
</thead>
<tbody>
<tr>
<td>“G”</td>
<td></td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Low power</th>
<th>Communication Infrastructure</th>
</tr>
</thead>
<tbody>
<tr>
<td>“LP”</td>
<td></td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Analog MS/RF/BCD</th>
<th>Consumers</th>
</tr>
</thead>
<tbody>
<tr>
<td>/Derivatives</td>
<td></td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Wireless</th>
<th>Automotive</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Multi segment</th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
</tr>
</tbody>
</table>
Technology Platform KPI

- High Performance
- General Purpose
- Low power
- Analog MS/RF/BCD/Derivatives

Key Performance Indicators (KPIs):
- Performance
- Power leakage
- Cost of ownership
- Area scaling
- Design simplicity
Technology R&D/MFG Leadership Brings

### Time-to-Market
- First device tape out in most advanced partner Fab.
- Device volume and yield ramp up thru fast learning technics.

### Innovation
- Device performance, power, area scaling.
- Device Add on.
- Cost-of-ownership, design simplicity

### Supply-Chain Multi Sourcing
- Time-to-Market first source
- Second /Alternative source thru Manufacturing Synchronization.

### Sustainable Effort
- cooperative model allows leveraged capture of technology innovation with risk mitigation.
- Shared capital/operating expenses thru cooperative/distributed model.
Outline

- Identifying the fundamental post-recovery market changes:
  - uncovering the new driving applications
- Understanding the crucial benefits of technology leadership

- A case study:
  ST Leadership in Technology & ST Competitive Advantage
Wireless: multi-purpose Products
“Phones”: High Performance @ Low Power

- Battery life
- Packaging (heat dissipation)
- Energy efficiency (environment)

Smartphone Tablets

Nova A9600 (28 nm) dual-core Eagle A15 at 2.5 GHz + 20X graphics improvement*

DA TE - March 2011

19

Feature phone

Nova A9540 (32 nm) dual-core A9 @ 1.85 GHz + 4X graphics improvement* Sampling 2011.

Basic phone

Nova A9500 (45 nm) dual-core A9 @ 1.2 GHz + 20% graphics improvement* Available

Multimedia convergence
- User experience
- Interfaces options
- Connectivity


DATE - March 2011
ST/ Networking ASICs
A growing SOC integration / Power Challenge

32nm LPH
- 400-900MHz
- 10-90W

28nm LPG
- >1GHz
- >40W avg.

65nm LP & LPGP
- 300-600MHz
- 10-80W

90nm
- 200-500MHz
- 15-70W

SerDes Roadmap
- Courtesy R Ferrari, G Cesana, ST

DATE - March 2011

STMicroelectronics

50+ Mgate
- 400-500 mm²

20-40 Mgate
- 200-400 mm²

5-20 Mgate
- 100-200 mm²

5 Mgate
- 50-100 mm²

>1GHz
>40W avg.

20nm
ST/Consumer relentless integration

Gen. 1
- 3 CPU’s, 250MHz, ~3W, Hier. Design, Wire bonding
- STB, IPTV & TV: Dual HD decode, DDR2, Analog
- STB, IPTV: HD format, Single decode, DDR1, Security, Analog

Gen. 2
- 5 CPU’s, 500MHz, ~3-4W, WB, FE integration
- STB, IPTV & TV: Decode+encode, DDR2/3, Graphic and 3DTV
- 65/55LP, 2005-2011

Gen. 3
- 6 CPU/GPU’s, 700MHz, ~3-6W, WB&FC, system Co-design
- STB, TV, Gateways: Decode+encode, DDR2/3, Graphic and 3DTV
- 40LP, 2008-2011

Gen. 4
- 8 CPU/GPU’s, 1-2GHz, ~3-7W, FC, system on single package
- DDR3 Systems: Digital platform with apps
- 10 CPU/GPU’s, >2GHz, ~3-7W, Flip Chip/3Dstack
- Heterogeneous
- PMIC
- Network

25-40k DMIPS « ARM based »
- 8-20k DMIPS « A9 based »

1k DMIPS « SH4 »

2k DMIPS « SH4 + »

Courtesy D Henoff, ST/HED

DATE - March 2011
A Distributed & Cooperative R&D:

- Leveraging best innovation versus:
  - Targeted product
  - Critical decision factor
  - Technology

- Mitigating risks of choice
- Sharing expenses effort
Value-Chain Management : Technology Innovation

- **Technology Innovation** leveraging bi/multi third parties competence centers:

  - Fundamental/advanced R&D thru joint Academia/Research Institutes Cooperation. (CEA LETI being the corner stone.)

  - Advanced CMOS both Low Power and General Purpose R&D thru ISDA (Advanced R&D pre T0).
Technology Operations balanced between internal/third parties competence centers:

- Advanced CMOS thru International Semiconductor Development Alliance (ISDA) with strong concurrent development activities.

- CMOS Analog and Derivatives thru internal Cluster of Crolles (France)

- Smart Power/Analog thru internal Cluster of Agrate (Italy)

- Distributed Design Enablement thru internal clusters of Agrate/Crolles/Greater Noida (India).
**Scope:** Electrical Synchronization of partner fabs to IBM
- Parametrical equivalence, GDS2-level
**Contract:** JDA between IBM and partners on 32LP Bulk and 28LP.
**Timing:** Program started 2H09 (28LP), end DEC2011.

**IP circuits Equivalence**
Direct validation between ST & foundry, not in Fabsync

**Parametrical Equivalence**
Equivalence to model
Model to silicon correlation

**In line Cp/Cpk Equivalence**
Metrology (SEMCD, Overlay, thin films, material composition) matching

**Test vehicle**
Common modeling macros
Common electrical monitoring

**Process**
FEOL & BEOL critical process steps,
Construction Analysis

DATE - March 2011
**ST Clusters of Competence**

**CROLLES/ROUSSET**
- Technology Development:
  - CMOS Core logic
  - Analog MS/RF, eDRAM, eNVM
  - CMOS Imaging
- Central CAD & Design Solutions

**AGRATE/CASTELLETTO**
- Technology Development:
  - Analog (BCD, HVCMOS)
  - MEMS
- Central CAD & Design Solutions

**TOURS & CATANIA**
- Technology Development:
  - Advanced Power Discretes
  - Micro fuel cell, solar, thin films batt.
  - Biotechnologies & healthcare
  - Integrated active & passive devices
- Specific CAD & Design Solutions

**GREATER NOIDA**
- Central CAD & Design Solutions
- Information & Communication Technology
Enabling performance race on products:
STE 32nm 1.5GHz Low Power A9 Core

- L1 Cache designed to reach 1.8GHz
- High Density L2 cache designed for 0.6 V Retention
- Faster pipelined Memory BIST Architecture
- Dedicated algorithms for Memory Test in 32/28nm
- Several IP/Lib Patents Pending
- High Performance Clock Generator
- Fast FF library designed for improving R2R performance in critical paths
- Power Switches: Peripheral Switches and Distributed Switches for best Vdrop.

DATE - March 2011
V_{dd} Scaling and energy efficiency
Scaling driven by process technology (T_{ox})

Power Supply

- 5V
- 4V
- 3V
- 2V
- 1V

High Voltage Solutions
- Mission Mode
- Thermal Management
- Supply Noise Management

Application / System Solutions
- SW control
- multiple OPP
- Closed loop AVS

Energy Efficient Design for +/- nominal V_{PP}

Low Voltage / Power Solutions
- Technology: Multi Vt / Large-L / BB
- SRAM: 6T -> 8T/ 0.5V SRAM
- Logic: Low VDD Logic / Async Logic
- IC Design: Design for Variability, GALS, AVS, ABB

STMicroelectronics

DATE - March 2011
V$_{dd}$ Scaling and energy efficiency

Keeping leakage under control

Power Supply

5V
4V
3V
2V
1V


Power Management
LP/GP Process
Multi Vt CMOS
Process compensation
HKMG

System Level Power Management

Product Leakage (a.u.) (no management)
CMOS 32/28nm: ST Differentiating Factors

ST offering process/IP add-ons vs. standard ISDA offer

**Cu Pillar**
- \(< 50\text{um Bump Pitch}\)
- Enabling 3D integration

**SP Bitcell for ARM Cache**
- \(0.244\mu\text{m}^2\) bitcell
- High current, low leakage, low Vdd
- 1.5GHz+ cache operation @ SS/1.0V/0C/Rcmax
- 0.6V Vmin RAM operation enabled

**MIM Decoupling Cap**
- Enhanced power supply control
- For GHz+ operation

**LPG & Poly Biasing**
- Specific High Speed Transistor (G) for critical paths inside Core
- High efficiency in overdrive mode
28nm FDSOI: the next speed booster
VLSI Platform Worldwide clusters

**DATE** - March 2011
Technology Leadership : Leading Edge

DATE - March 2011
ST Technology Leadership

- **ST R&D cooperative model** allows leveraged capture of technology innovation and risk mitigation.

- **ST leadership in technology** enables differentiated / competitive product positioning through:
  - Device Integration
  - Device add-on for Derivatives / Analog
  - Design Enablement
  - Specific process modules for best device performance
  - Fast yield learning cycle time techniques

and a full multi sourcing supply-chain efficiency.
What’s next after 20nm?

- High Performance (μPs) will move to 15nm with relaxed design rules
- SOC/ASICs (LP/GP) will move to 14nm for dense rules because 2x shrink factor, +30% Perf vs 20nm
- 2 main disruptions are expected:
  - Lithography: moving from 193nm immersion to EUV
  - Device: moving from bulk CMOS to Thin Silicon devices
- For devices, 2 options:
  - FinFET
  - FDSOI
- 3D integration could appear faster
Main candidates after bulk are FinFET and FDSOI:

<table>
<thead>
<tr>
<th></th>
<th>FDSOI</th>
<th>FinFET</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Strengths</strong></td>
<td>- 2D (planar) process</td>
<td>- Double gate: Electrostatic control</td>
</tr>
<tr>
<td></td>
<td>- Electrostatic control</td>
<td></td>
</tr>
<tr>
<td><strong>Risk</strong></td>
<td>- Compatibility with</td>
<td>- Process complexity (3D)</td>
</tr>
<tr>
<td></td>
<td>conventional « performance boosters »</td>
<td></td>
</tr>
<tr>
<td></td>
<td>- Compatibility with</td>
<td>- Compatibility with conventional « performance boosters »</td>
</tr>
<tr>
<td></td>
<td>conventional « performance boosters »</td>
<td></td>
</tr>
</tbody>
</table>
Transistor Architecture Trends

32/28nm

- Fully Depleted SOI with Hybrid Bulk
- Gate First Metal Gate High-K
- 28nm Low Power (ST/IBM IEDM 2009)

22/20nm

- Bulk w/ enhanced stressors
- 2nd Generation MGHK (Gate Last)
- Improved junctions
- Fully Depleted SOI with Ultra Thin BOX and Stressors

16nm/14nm

- FinFETs
- Fully Depleted SOI with Hybrid Bulk
- 25nm FDSOI (ST/IBM VLSI 2010)
- 15nm FDSOI (ST/LETI VLSI 2010)

11nm/10nm

- Record Performance Nanodot FET (ST VLSI 2009)
- HQS GAA Devices (ST IEDM 2010)

8nm/7nm

- Self Aligned Planar Double Gates structures

DATE - March 2011
Next to come: 3D, Photonics

- 3D/Heterogeneous Integration of Wide-IO DRAM
- Benefits: Low-Power DRAM/SOC data connexion
- Challenges: cost, thermal management, Test, Supply Chain

Communication bandwidth rapidly increasing from few Gb/s to 100Gb/s.

- Copper wire technology not able to sustain such data rates
- Photonics on silicon technology allows die to die and within die optical communication

Photonics on Silicon
SOC CMOS Application Trends: Summary

- SOC Applications require high-performance energy-efficient Processing Units (CPUs, GPUs, …):  
  - Wireless  
  - Consumer  
  - Automotive  
  - Computer Peripherals

- ST’s 32/28nm LP / Design Platform at state-of-the-art  
  - Process optimizations, above industry leading ISDA HKMG 32nm  
  - Library/IP design  
  - CAD Flow/ Sign-off optimization  
  - Application-driven

- Partnerships are key to optimize R&D investment  
  - Process, IP, Design, EDA, Universities, Labs
Mastering the Technology Platform

- Speed
- Area
- Power
- Cost

Technology
Sys. Architecture
IP / Library
Methodology

SoC Designers
VLSI Design Platform
Silicon Technologies
ST has proven the competitive advantage of its R&D model at 40nm then at 28 nm node.

Moving to 20 nm and beyond, with increasing complexity, facing major architecture, process, equipment disruptions.

Yet investing deep knowledge in Process, Design Enablement, Manufacturing and their interactions,

ST will strengthen its position of

‘UNDISPUTED LEADER IN MULTI MEDIA CONVERGENCE AND SENSE&POWER APPLICATIONS’