Abstract

Research activities of the electronic engineering department are concerned with Algorithm-Architecture-Matching approach for iterative processing (“turbo” principle) in the digital communications systems. The turbo principle is a general way of processing data in receivers so that no information is wasted. Our work is about all aspects of mapping algorithms to architectures to implementations. Two prototypes are presented: a 5Gb/s experimental setup for turbo decoding of a $(31,29)^2$ RS product code and a flexible multi-ASIC NoC-based FPGA prototype for convolutional turbo decoding.

1. Introduction

Rapid prototyping is an important step in the development and verification of complex digital communication systems. The goal is to replace time-consuming simulations based on abstract models of the system with real-time experiments under real-world conditions. In our department, new hardware architectures corresponding to iterative receiver algorithms are thus implemented in a real-time platform using FPGA. The experimental setup is composed of a Dinigroup board [1] that includes six Xilinx Virtex-5 LX330 FPGAs. A Xilinx Virtex-5 LX330 FPGA contains 51,840 slices that can emulate up to 12 million gates of logic. It should be noted that Virtex-5 slices are organized differently from previous generations. Each Virtex-5 slice contains four Look Up Tables (LUTs) and four flip-flops instead of two LUTs and two flip-flops in previous generation devices. The board is hosted on a 64-bit, 66MHz PCI bus that enables communication at full PCI bandwidth with a computer. Architectures for two research projects have been implemented in this platform. The two experimental prototypes are detailed in the rest of this paper.

2. Prototyping of a $(31,29)^2$ Reed-Solomon Turbo Decoder processing at 5-Gb/s

Block Turbo Codes (BTC), also known as Turbo Product Codes (TPC), are next-generation Forward Error-Correction (FEC) codes that offer an interesting alternative to classical convolutional Turbo Codes for applications requiring either high code rates ($R > 0.8$), very low error floors, or low-complexity decoders able to operate at several gigabits per second. A full-parallel architecture for the turbo decoding of product codes was proposed in [2]. The major advantage of this full-parallel architecture is that it enables the memory block between each half-iteration to be replaced by simple interconnection networks. In this context, the use of single-error-correcting Reed-Solomon (RS) product codes was investigated in an ultra high-speed context. The purpose of the prototype is to demonstrate that Reed-Solomon turbo decoders can effectively achieve information rates above 1Gbps. To the authors’ knowledge, this is the first implementation of FEC decoder onto an FPGA target at information throughputs superior to 1Gbps. Figure 1 shows the different components of the digital communication setup implemented onto six FPGAs.

Figure 1: 5Gb/s experimental setup for turbo decoding of a $(31,29)^2$ RS product code
One FPGA is allocated to the component implementation of the transmission part. Each of the five other FPGAs is dedicated to the implementation of one decoding iteration. A decoding module corresponds to a full-parallel architecture dedicated to the decoding of a matrix of 31 x 31 coded soft values. 1,550 bits have to be exchanged between the decoding modules during each clock period \( f_{cl}=37.5\text{MHz} \). The board offers 200 chip to chip LVDS for each FPGA to FPGA interconnect. Unfortunately, this number of LVDS is insufficient to enable the transmission of all the bits between the decoding modules. To solve this implementation constraint, we have chosen to add SERializer/DESerializer (SERDES) modules for the parallel-to-serial conversions and for the serial-to-parallel conversions in each FPGA. SERDES modules are clocked with \( f_s = 8f_{cl} = 300\text{MHz} \) and operate at 8:1 serialization or 1:8 deserialization. Thanks to 200 chip to chip LVDS and the SERDES modules, data are exchanged between the different FPGAs at a throughput of 58,125Gb/s while the working frequency and the information data rates are only 37.5MHz and 5Gb/s, respectively. As the hardware emulation speeds up the simulation by a few orders of magnitude, prototype performance has been measured until a BER of \( 10^{-15} \).

3. Prototyping of a multi-ASIP NoC-based architecture for turbo decoding

Current and emerging wireless communication standards impose the use of various forward error-correction techniques with diverse parameters in terms of code rate and frame length and severe requirements in terms of throughput and error rate. This is particularly the case regarding convolutional turbo codes. Single and double binary constituent convolutional codes are proposed in the standards with various code structures, code rates from 1/3 to 6/7, frame size from 40 to 20736 bits, diverse interleaving schemes, and increasing throughout requirement.

Flexibility and high-throughput requirements are being widely investigated in this application domain during the last few years. Several implementations have also been proposed. Some of these implementations succeeded in achieving high throughput for specific standards with a highly dedicated architecture. However, these implementations do not take into account flexibility and scalability issues. Conversely, others implementations include software and/or reconfigurable parts to achieve the required flexibility while achieving much lower throughput.

In order to tackle flexibility and performance requirements simultaneously, multi-core and Application-Specific Instruction-set Processor (ASIP) based implementations are being proposed as promising inevitable candidate.

In the presented prototype (Figure 2) we demonstrate a multi-ASIP and Network-on-Chip (NoC) based platform for high throughput flexible parallel turbo decoding. This implementation is achieved using an ASIP with Single Instruction Multiple Data (SIMD) architecture and a specialized and extensible instruction-set [3]. The proposed ASIP integrates two identical BCJR computation units, corresponding to forward and backward processing in the MAP algorithm. It was developed in LISA language and generated automatically using the Processor Designer framework from CoWare. Multiple ASIP are interconnected through a Butterfly-based NoC [4] exploiting sub-block and components decoder parallelism levels.

![Multi-ASIP NoC-based prototype for high throughput flexible convolutional turbo decoding](image)

The major characteristics of the proposed platform are its flexibility and scalability which make it reusable for all simple and double binary turbo codes of existing and emerging standards. Results obtained for double binary WiMAX turbo codes demonstrate around 50 Mbps throughput with an 8-ASIP prototype occupying 46% of a single Virtex-5 LX330 FPGA.

4. References


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