### UB11 Session 11

**Date:** Thursday, March 30, 2017  
**Time:** 14:30 - 16:30  
**Location / Room:** Booth 1, Exhibition Area

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| UB11.1 | TGV: TESTER GENERIC AND VERSATILE FOR RADIATION EFFECTS ON ADVANCED VLSI CIRCUITS | Miguel Solinas, TIMA, FR  
Alexandre Coelho Coelho, Juan Fraire, Nacer Eddine Zergainoh and Raoul Velazco, Univ. Grenoble Alpes, CNRS, Grenoble INP, FR |
| UB11.2 | NETFI-2: AN AUTOMATIC METHOD FOR FAULT INJECTION ON HDL-BASED DESIGNS | Miguel Solinas, Juan Fraire, Nacer-Eddine Zergainoh, Pablo Ferreyra and Raoul Velazco, TIMA, FR  
Alexandre Coelho, Université Grenoble Alpes, FR |
| UB11.4 | AF3-MC: DEVELOPMENT OF MIXED CRITICALITY SYSTEMS USING MBSE | Johannes Eder and Sebastian Voss, fortiss, DE  
Thomas Boehm, fortiss, DE |
| UB11.5 | A VOLTAGE-SCALABLE FULLY DIGITAL ON-CHIP MEMORY FOR ULTRA-LOW-POWER IOT PROCESSORS | Jun Shimori, Kyoto University, JP  
Toshu Ishihara and Hitoshi Onodera, Kyoto University, JP |
| UB11.6 | GNHC: AN ULTRA-FAST, HIGHLY EXTENSIBLE, CYCLE-ACCURATE GPU-BASED PARALLEL NETWORK-ON-CHIP SIMULATOR | Amir CHARIF, TIMA, FR  
Nacer-Eddine Zergainoh and Michael Nicolaidis, TIMA, FR |
UB11.7 EMU: RAPID FPGA PROTYPING OF NETWORK SERVICES IN C#

Presenter:
Salvator Galea, University of Cambridge, GB

Authors:
Nik Sultana\textsuperscript{1}, Pietro Bressana\textsuperscript{2}, David Greaves\textsuperscript{1}, Robert Soulé\textsuperscript{2}, Andrew W Moore\textsuperscript{1} and Noa Zilberman\textsuperscript{1}

\textsuperscript{1}University of Cambridge, GB; \textsuperscript{2}Università della Svizzera italiana, CH

Abstract
General-purpose CPUs and OS abstractions impose overheads that make it challenging to implement network functions and services in software. On the other hand, programmable hardware such as FPGAs suffer from low-level programming models, which make the rapid development of network services cumbersome. We demonstrate Emu, a framework that makes use of an HLS tool (Kiwi) and enables the execution of high-level descriptions of network services, written in C#, on both x86 and Xilinx FPGA. Emu therefore opens up new opportunities for improved performance and power usage, and enables developers to more easily write network services and functions. We demonstrate C# implementations of network functions, such as Memcached and DNS Server, using Emu running on both x86 and NetFPGA-SUME platform and show that they are competitive to natively written hardware counterparts while providing a superior development and debug environment.

UB11.9 HEPSCODE: A SYSTEM-LEVEL METHODOLOGY FOR HW/SW CO-DESIGN OF HETEROGENEOUS PARALLEL DEDICATED SYSTEMS

Presenter:
Luigi Pomante, University of L'Aquila, IT

Authors:
Giacomo Valente\textsuperscript{1}, Vittoriano Muttillo\textsuperscript{1}, Daniele Di Pompeo\textsuperscript{1}, Emilio Incerto\textsuperscript{2} and Daniele Ciambrone\textsuperscript{1}

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Abstract
Heterogeneous parallel systems have been recently exploited for a wide range of application domains, for both the dedicated (e.g. embedded) and the general purpose products. Such systems can include different processor cores, memories, dedicated ICs and a set of connections between them. They are so complex that the design methodology plays a major role in determining the success of the products. So, this demo addresses the problem of the electronic system-level hw/sw co-design of heterogeneous parallel dedicated systems. In particular, it shows an enhanced CISP/SystemC-based design space exploration step (and related ESL-EDA prototype tools), in the context of an existing hw/sw co-design flow that, given the system specification and related F/NF requirements, is able to (semi)automatically propose to the designer: - a custom heterogeneous parallel architecture; - an HW/SW partitioning of the application; - a mapping of the partitioned entities onto the proposed architecture.

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