International Workshop on Optical/Photonic Interconnects for Computing Systems (OPTICS Workshop)

Session Type: Workshop
Date: Friday, March 13, 2015
Time: 08:30-16:30
Location / Room: Sept Laux 5

URL: Proceedings (Available for attendees only! The password has been sent to you by email or you may ask for the password at the on-site registration desk) [1]
Call [2]

General Chairs
Gabriela Nicolescu, Polytechnique Montréal, CA (Contact Gabriela Nicolescu [3])
Jiang Xu, Hong Kong University of Science and Technology, CN (Contact Jiang Xu [4])
Sébastien Le Beux, Lyon Institute of Nanotechnology, Ecole Centrale de Lyon, FR (Contact Sébastien Le Beux [5])

Programme Committee Chair
Mahdi Nikdast, Polytechnique Montréal, CA (Contact Mahdi Nikdast [6])

Invited Speakers
Antonio La Porta, IBM, Zurich Research Laboratory, CH (Contact Antonio La Porta [7])
Davide Bertozzi, University of Ferrara, IT (Contact Davide Bertozzi [8])
Fabiano Hessel, PUCRS, BR (Contact Fabiano Hessel [9])
Ian O’Connor, Lyon Institute of Nanotechnology, FR (Contact Ian O’Connor [10])
John Ferguson, Mentor Graphics Corp, US (Contact John Ferguson [11])
José Flich, Universidad Politecnica de Valencia, ES (Contact José Flich [12])
Olivier Sentieys, INRIA - University of Rennes 1, FR (Contact Olivier Sentieys [13])
Sandro Bartolini, Università di Siena, IT (Contact Sandro Bartolini [14])
Sébastien Cremer, STMicroelectronics, FR (Contact Sébastien Cremer [15])
Yaoyao Ye, Huawei Technologies Co. Ltd., CN (Contact Yaoyao Ye [16])
Yvain Thonnart, CEA, LETI, MINATEC, FR (Contact Yvain Thonnart [17])

Scope of the Workshop and Target Audience
Multiprocessor System-on-Chip (MPSoC) is becoming the standard for high-performance computing systems. The performance of an MPSoC is determined not only by the performance of its processing cores and memories, but also by how efficiently they collaborate with one another. As the technology advances and allows the integration of many processing cores, metallic interconnects in MPSoCs will consume significant power while imposing high latency and low bandwidth. Shifting to the many-core era necessitates considering an alternative interconnect technology to replace the traditional electrical interconnects. Among such technologies, photonic technology has demonstrated promising potentials to address the aforementioned issues with the metallic interconnects in MPSoCs. In this context, high-performance silicon photonic devices, which are CMOS compatible, are necessary to construct photonic interconnect networks. Furthermore, it is required to explore the feasibility and performance of photonic interconnects as well as the guidelines and design requirements to realize such interconnects.

OPTICS aims at discussing the most recent advances in photonic interconnects for computing systems, covering topics from the device fabrication all the way up to the system level design. The workshop is of interest to researchers working on silicon photonics and high-performance computing systems. It is comprised of invited talks of the highest caliber in addition to refereed paper presentations. Industry’s and academia’s views on the feasibility and recent progresses of optical interconnects will be discussed during the workshop.

Topics to be discussed in the workshop include (but are not limited to) the following:

- **Design Methodology, Modelling and Tools**: design space exploration, optimization, thermal-aware design, floor-planning, system level modeling and simulation.
- **Architecture/Micro-Architecture**: hybrid optical-electronic interconnects, passive/active-based optical switches networks, communication protocols.
- **Applications**: high-performance computing, photonics interconnect for memory.
- **Silicon Photonics Devices**: circuit demonstrator, on-chip lasers, photodetectors, electro-optic modulators, optical switches, athermal devices.
- **Silicon Photonics Circuits**: optical switches and routers, high-bandwidth I/O.

Paper Submission
You are invited to participate and submit your contributions to OPTICS. Submissions should be in the standard IEEE 2-column conference format, and they should not exceed four pages in length, including all the figures, tables, and references. Submissions must be sent to the program chair before the submission deadline. This workshop does not require blind submissions. All submissions will undergo a peer-review process and accepted papers will be presented at the workshop as short oral presentations in one of the regular sessions. Informal proceedings with accepted papers will be made available at the end of the workshop. Please note that the accepted papers will NOT disseminated through the official DATE proceedings or through any other formal channels, such as, for example, the IEEEExplore or the ACM Digital Library. Therefore, authors are free to submit their work to other archival conferences and journals.

Important Dates
Submission deadline: 23rd Nov. 2014 23rd Nov. 2014
Acceptance notification: 10th Dec. 2014 10th Dec. 2014
Final program: 4th Dec. 2014
Camera ready: 15th Jan. 2015

Confirmed Invited Speakers
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<tr>
<th>Time</th>
<th>Label</th>
<th>Session</th>
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<tr>
<td>08:30</td>
<td>W09.1</td>
<td>Introduction</td>
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<td>Chair: Gabriela Nicolescu, Ecole Polytechnique de Montreal, CA, Contact Gabriela Nicolescu [3]</td>
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<tr>
<td>08:30</td>
<td>W09.1.1</td>
<td>Introduction to OPTICS workshop</td>
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<td></td>
<td>Gabriela Nicolescu¹ and Mahdi Nikdast²</td>
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<td>¹Ecole Polytechnique de Montreal, CA; ²Ecole Polytechnique de Montréal, CA</td>
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<td>08:40</td>
<td>W09.2</td>
<td>Morning Session on System Design, Architecture, Modelling, and Applications</td>
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<td>Chair: Sébastien Le Beux, Lyon Institute of Nanotechnology, Ecole Centrale de Lyon, FR, Contact Sébastien Le Beux [5]</td>
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<tr>
<td>08:40</td>
<td>W09.2.1</td>
<td>Scalable Optical Interconnects for Computing Systems and the Need for Electro-Optical Integration</td>
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<td>Antonio La Porta, IBM, Zurich Research Laboratory, CH</td>
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<td>09:15</td>
<td>W09.2.2</td>
<td>Towards a Vertically Integrated Synthesis Flow for Predictable Design of Wavelength-Routed Optical NoCs</td>
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<td>Davide Bertozzi, University of Ferrara, IT</td>
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<td>09:35</td>
<td>W09.2.3</td>
<td>Inter/Intra-Chip Optical Networks: Opportunities and Challenges</td>
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<td>Jiang Xu, Hong Kong University of Science and Technology, CN</td>
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<td>09:55</td>
<td>W09.2.4</td>
<td>A Force-Directed Placement Algorithm for 3D Optical Networks-on-Chip</td>
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<td>Anja von Beueningen and Ulf Schlichtmann, Technische Universität München, DE</td>
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<td>10:15</td>
<td>W09.2.5</td>
<td>System-Level Design Space Exploration for SoCs Integrating Optical Networks on Chip</td>
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<td>Fabiano Hessel, Pontifícia Universidade Católica do Rio Grande do Sul, BR</td>
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<td>10:35</td>
<td>W09.2.6</td>
<td>Coffee break</td>
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<td>11:00</td>
<td>W09.2.7</td>
<td>Meet in the Middle: Leveraging Optical Interconnection Opportunities in Chip Multi Processors</td>
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<td>Sandro Bartolini, Università di Siena, IT</td>
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<td>11:20</td>
<td>W09.2.8</td>
<td>Electronic vs Photonic NoCs: Should They Compete or Collaborate?</td>
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<td>José Fich, Universidad Politécnica de Valencia, ES</td>
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<td>11:40</td>
<td>W09.2.9</td>
<td>Bandwidth Requirements in Manycore Architectures: What Can 3D Bring?</td>
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<td>Olivier Sentieys, INRIA - University of Rennes 1, FR</td>
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<td>12:00</td>
<td>W09.2.10</td>
<td>Lunch</td>
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<td>13:00</td>
<td>W09.3</td>
<td>Afternoon Session on Silicon Photonics Devices, Circuits, and Challenges</td>
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<td>13:00</td>
<td>W09.3.1</td>
<td>Building a Scalable Design Environment for Silicon Photonics through PDKs</td>
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<td>John Ferguson, Mentor Graphics Corp, US</td>
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<td>13:35</td>
<td>W09.3.2</td>
<td>Recent Development of Si-Photonics in 300mm Fab</td>
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<td>Sebastien Cremer, STMicroelectronics, FR</td>
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13:55 W09.3.3 Silicon Photonics for Interposer
Yvain Thomart, CEA, LETI, MINATEC, FR

14:15 W09.3.4 Thermal Management of Optical Interconnects
Yao Yao Ye, Huawei Technologies Co. Ltd., CN

14:35 W09.3.5 Coffee break

15:00 W09.3.6 Parametric Exploration of Vertical Tapered Coupler for 3D Optical Interconnection
Romain Schuster¹, Alberto Parini² and Gaetano Bellanca²
¹Telecom Bretagne, Campus Brest, FR; ²University of Ferrara, IT

15:20 W09.3.7 The Last Mile? Remaining Challenges in Optical Interconnect
Ian O’Connor, Lyon Institute of Nanotechnology, FR

15:30 W09.4 Panel
Moderator:
Ian O’Connor, Lyon Institute of Nanotechnology, FR, Contact Ian O’Connor [10]

15:30 W09.4.1 Panel discussion
John Ferguson¹, Antonio La Porta², Gabriela Niculescu³, Olivier Sentieys⁴, Davide Bertozzi⁵ and Jiang Xu⁶
¹Mentor Graphics Corp, US; ²IBM, Zurich Research Laboratory, CH; ³Ecole Polytechnique de Montreal, CA; ⁴INRIA - University of Rennes 1, FR; ⁵University of Ferrara, IT; ⁶Hong Kong University of Science and Technology, CN

16:20 W09.5 Concluding Remarks and Closing Session
Chair:
Sébastien Le Beux, Lyon Institute of Nanotechnology, Ecole Centrale de Lyon, FR, Contact Sébastien Le Beux [5]

16:20 W09.5.1 Concluding remarks
Sébastien Le Beux, Lyon Institute of Nanotechnology, Ecole Centrale de Lyon, FR

16:30 W09.5.2 Closing

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