**4.8 State-of-the-art in Verification: European Tertulia IC Design - Enabling AMS Structured Verification / Verification in FPGA & IP design flows**

**Date:** Tuesday, March 25, 2014  
**Time:** 17:00 - 18:30  
**Location / Room:** Exhibition Theatre  
**Organiser:** Andreas Brüning, Silicon Saxony, DE

### 17:00  4.8.1 BRING ASIC-ALIKE VERIFICATION TO YOUR FPGA & IP DESIGN FLOW

**Speaker:** Scott Calkins, Blue Pearl Software Inc, US  
**Abstract**  
This talk will highlight how successful design teams and IP firms such as PLDA are able to develop high quality code by using a process to control and optimize the HDL which is developed by different designers in different locations, even those with varying skill sets. PLDA designs and sells intellectual property (IP) cores and prototyping tools for ASIC and FPGA that aim to accelerate time-to-market for embedded electronic designers. PLDA specializes in high-speed interface protocols and technologies such as PCIe. Through the use of Blue Pearl Software's Symbolic Engine that maps code to RTL level, then analyzes it for known structures, PLDA is able to generate deterministic results for the handful of synthesizers and target fabrics their customers demand. Analyzing the HDL before it is brought into cycle-based simulators allows designers to run FPGA-centric structural checks for Xilinx and Altera so it helps to detect bugs and specific optimizations earlier in the flow and automatically for the success and satisfaction of our customer's designers: "Blue Pearl Software's design analysis tool enables integration of formal verification techniques to our design flow, in order for us to detect structural bugs at the very early stage of code integration, and thus to deliver highest quality IP to our customers. On top, we definitely recommend Blue Pearl Software's solution to anyone who needs to increase design team productivity." Hugues Deneux, R&D Director of PLDA

### 17:20  4.8.2 TOWARDS CO-DESIGN AND CO-VERIFICATION OF HW, SW, AND ANALOG SYSTEMS

**Speaker:** Christoph Grimm, TU Kaiserslautern, DE  
**Abstract**  
We can today design and verify digital hardware and software in a way that deserves the word co-design. Co-design achieves a significantly higher productivity in the design, and better performances of the product. Unfortunately, co-design and co-verification is not yet done in a similar productive way for analog and RF systems. The presentation will give an overview of methodology, tools, and languages that include analog and RF design into a comprehensive co-design methodology. Particular focus is on tool integration and power profiling crossing the discrete-analog border.

### 17:40  4.8.3 ENABLING AMS STRUCTURED VERIFICATION

**Speakers:**  
Gunter Strube\(^1\) and Stefan Getzlaff\(^2\)  
\(^1\)MunEDA GmbH, DE; \(^2\)ZMDI, DE  
**Abstract**  
The verification of the robustness of design specifications with respect to all combinations of worst-case parameter conditions not only improves the design confidence, but it is increasingly becoming a requirement for quality assurance and documentation for norms. It is a complex task consuming significant man power and compute power and it tends to be sacrificed under time pressure in the final stage of a project. We present an automated structured approach that differentiates through its thoroughness, its efficiency and most of all it's ease-of-use. It enables even novice designers to apply advanced state-of-the-art statistical tools to create a report including a measure of robustness for each specification and for the circuit.

### 18:20  4.8.4 TERTULIA IC-DESIGN - EUROPE TEAMS UP

**Speaker:** Jürgen Haase, edacentrum, DE  
**Abstract**  
The clusters of Grenoble and Dresden developed to leading clusters of world-wide importance. Now these clusters have initiated substantial initiatives for collaboration in order to strengthen Europe's position in the world-wide competition of microelectronics sites. This talk gives an overview about actual initiatives - including the tertulia IC-Design.

### 18:30 End of session

**Exhibition Reception** in Several serving points inside the Exhibition Area (Terrace Level)  
The Exhibition Reception will take place in the exhibition area (Terrace Level). All exhibitors are welcome to provide drinks and snacks for delegates and visitors.

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