

Verific-MM: Systematized Verification Metrics Generation with UCIS for Improved Automation on Verification Closure

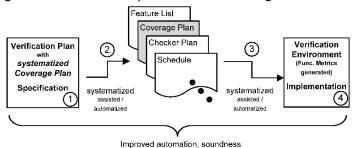


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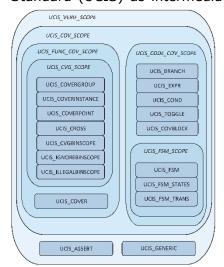
## FRAMEWORK FOR CONSISTENT VERIFICATION METRIC GENERATION

Verific-MM is an approach to systematize and accelerate the coverage plan engineering as well as the verification environment's (functional) metric code generation - usually a time-consuming and error-

prone task - for which little automation is available. In **Step (1)** we collect the coverage plan parts of the verification plan by means of a custom OMG RegIF meta model suitable for miscellaneous verification metrics, for example targeting functional coverage. **Step (2)** translates the metric information into a model instance of the Accellera Unified Coverage Interoperability



Standard (UCIS) as intermediate format. As UCIS can hold various coverage producers information it



During the simulation and regression runs we collect the verification metric results and annotate them back to the respective UCIS data model elements via a generated Set/Get API for the basic data elements structures of UCIS. In conclusion, our approach allows consistent construction and generation of verification metrics as well as result backannotation from/to a single source.

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also can be used *prior* to the actual simulation and regression runs to hold the metric information. In our approach UCIS acts not only as a common standardized data model for exchange and merge of coverage producers, but is efficiently used for processing the coverage plan from higher levels of abstraction. Step (3) binds the UCIS intermediate model to the design model by model mapping. This step relies on extraction of a design model of sufficient detail of the current DUT implementation status, e.g. by tools such as PINAPA. The concrete mapping requires knowledge about the verification intent and cannot be further automized. By means of AMW we provide assisted mapping of metric model elements with design elements. In Step (4) we generate appropriate verification metric code for the target language – e.g. IEEE-1666 SystemC, IEEE-1800 SystemVerilog or IEEE 1647 e - for the testbench environment, based on the mapped model information.

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## Acknowledgement

This work was partly funded by the German Ministry of Education and Research (BMBF) under IKT2020 through the project EFFEKTIV (01S13022) and ARAMIS (01IS11035). We greatly appreciate the cooperation with the project partners.

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