



PHARAON

Parallel and Heterogeneous Architectures for Real-time Applications

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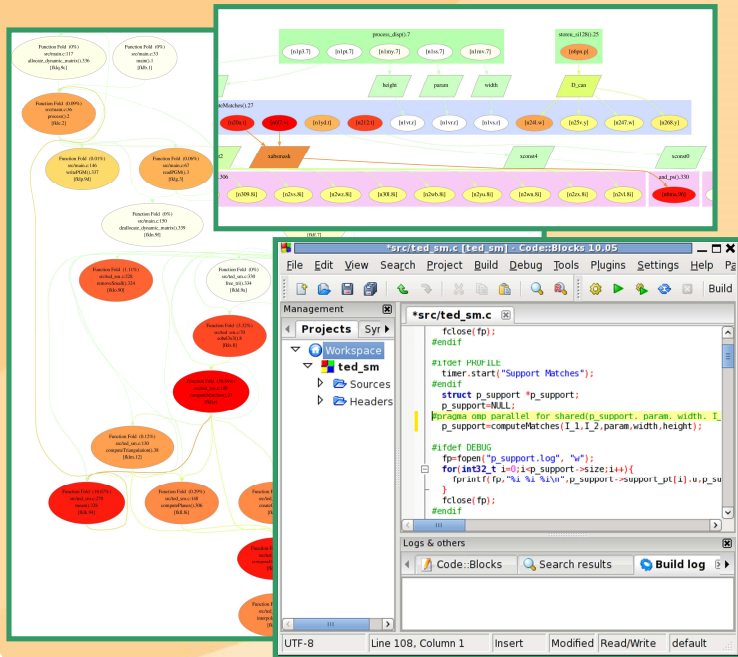
Objectives & Impact

Develop two sets of techniques and tools, aimed at exploiting low-power capabilities of embedded SoCs with heterogeneous CPU, DSP and GPU cores.

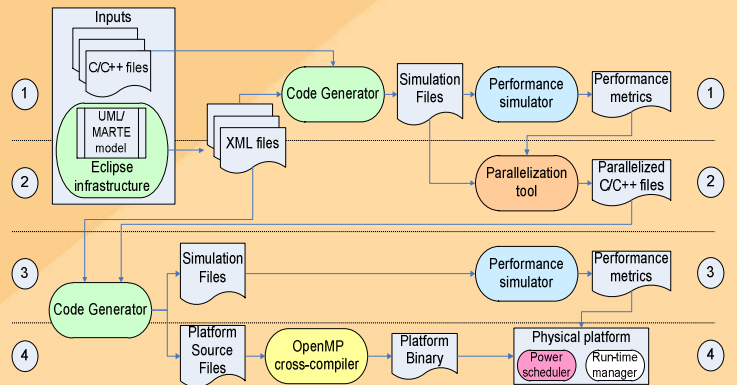
1. Find the most adequate software architecture taking into account hardware constraints.
 - analyze the parallel structure of an application
 - automatically generate multi-processor code.
2. Adapt the platform performance (e.g. frequency & voltage) to consume only the required energy.
 - run-time reconfiguration manager
 - low power scheduler.

Software parallelization

The legacy software to be parallelized is analyzed to identify and display (in a highly compacted form) data dependencies and opportunities for parallelization.



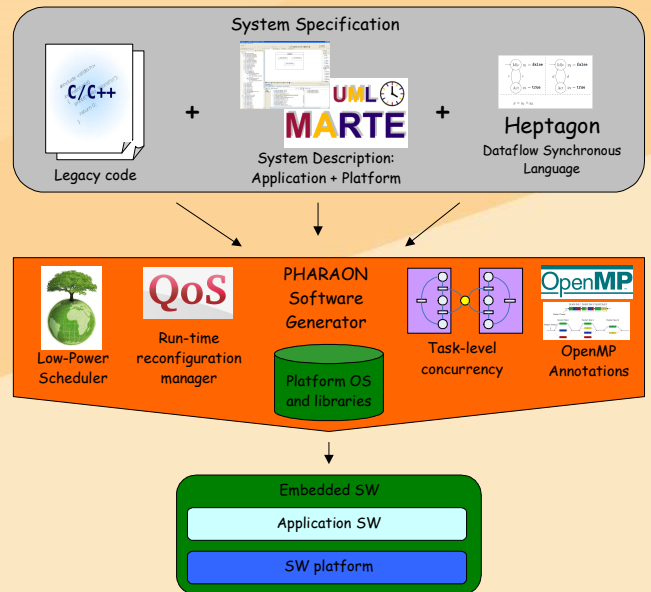
Design Flow



Code Generator

The complete SW stack to be executed in each node is automatically generated from the UML/MARTE models and the functional code.

The generator produces optimized code, including additional code providing parallelism and run-time optimizations.



Demonstrators

Three demonstrators from two domains: radio and image processing, are being produced.

Two radio demonstrators:

1. MAC layer implemented on a multicore ARM based platform
2. Physical layer (L1) with real-time reconfiguration and multi-stream capabilities implemented on an ARM-based platform with a specialized DSP

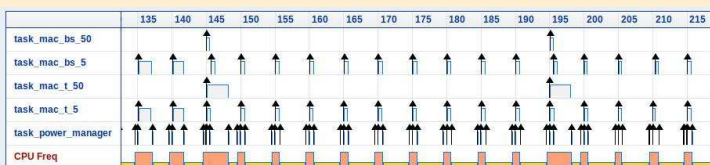


Image processing demonstrator:

3. Advanced 3D stereoscopic application with real-time and high definition constraints targeting the automotive domain for human and obstacle detection

