

RTL+ Design Environment: Walk Before You Run

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Abstract—To enable development of high level designs with hardware correspondence, synthesizability must be satisfied in a top-down manner. Thus in this work, instead of using TLM-2.0 which is not yet established for synthesis, we will start with a level above RT level, “RTL+”. RTL+ is basically using TLM-1.0 channels and includes abstract communications and handshakings that are mainly hidden from the high level designer. We have developed a package of SystemC channels with hardware correspondence (synthesizable HDL) for the communication between various cores (with simple interfaces) and standard buses.

I. RTL+ PACKAGE

Continuous growth in design complexity has led the designers to develop their designs at a higher level of abstraction to hide low level details and reduce design step complexity. Designers require the possibility of developing fully synthesizable designs by following certain design rules at a high level of abstraction. To enable this, synthesizability must be satisfied in a top-down manner. Although SystemC TLM-2.0 enables designers to describe high level designs, this standard has not been established for synthesis. In our work we propose a package, that we refer to as RTL+ that is one step above RTL and is fully synthesizable to RTL descriptions.

RTL+ enables designers to implement designs at a higher level of abstraction than RTL. RTL+ uses TLM-1.0 abstract channels to handle communications between functional units and standard busses. This capability enables designers to focus on the development of the behavior of the desired system and leaves communication details such as low level handshaking to the channels. After the design phase, the designer is provided with the HDL equivalent description of the design which is fully synthesizable with existing tools, and enables the designer to see and modify the RTL hardware description that is extracted from the high level design. RTL+ is aimed to move from TLM-1.0

toward TLM-2.0 and further toward actual system level design, therefore SystemC is used for its implementation.

RTL+ package includes the definition of functional modules, standard busses and the abstract channels that connect them. Functional modules have simple *Start* and *Done* interface signals but in some cases the handshaking may be more complex. The standard busses in this package cover a number of common busses like AMBA, Avalon, and Wishbone. For each standard bus we define abstract channels with various communication types including burst, FIFO, etc. All components are defined in SystemC and their corresponding synthesizable HDL descriptions are also available. This way, the designer will only develop the required units, choose a bus, and select the desired channel to handle the communications. The channel will automatically handle low level handshaking signaling as specified at the RTL+ level. Figure 1 shows the methodology of RTL+ library.

In the first phase of this work, the corresponding HDL description for the high level (at RTL+ level) design is created manually. This will further be improved to a design automation tool which automatically generates HDL description of the high level design. To demonstrate this project, we have developed a high level design of a typical system, and have provided the HDL description of the design. The system consists of a processor, instruction and data memories, and a number of dedicated arithmetic cores like Cordic processors. We use AMBA standard bus for communication between the modules, and have developed abstract channels corresponding to AMBA to connect system modules to the bus. The Cordic processors are enhanced with simple interfaces of *Start*, *Done* and *Busy* handshaking. This description of the system is translated to a corresponding HDL description of all modules, bus structures, and channels. The result of this step is a fully synthesizable RTL description.

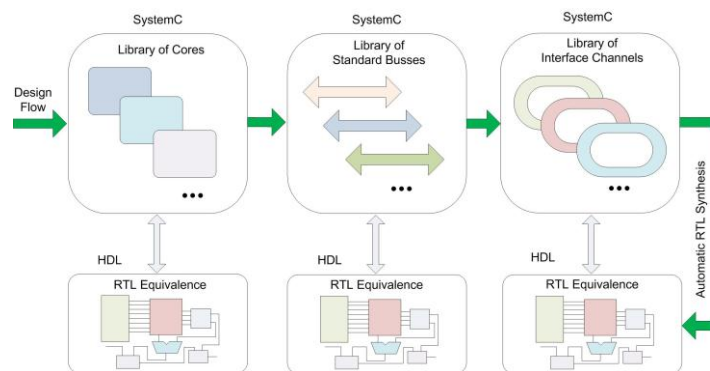


Figure 1. RTL+ Library and Methodology