

# HWDeblur – Design of a High Performance Core for Removing Blur Effect on Images

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## Abstract

*This work aims at developing a high performance FPGA-based IP-core able to perform a deblurring algorithm in real-time. Modern approaches to deblurring usually either only handle simple types of blur, or need heavy user interaction. Moreover, they usually require several minutes (or even whole hours) to process a single image. Our purpose is to study the current state-of-the-art and identify the best deblurring algorithms that are suitable for a hardware implementation. The selected algorithm is optimized and implemented in hardware in order to perform the deblurring task with highest possible performances.*

## 1. Introduction

The problem of restoring a blurry and/or noisy image has long been a challenging problem in digital imaging. It has been studied in depth in all its forms. However, a definitive solution to the problem has yet to be found. In fact, existing deblurring techniques either only handle simple types of blur, or need heavy user interaction. Moreover, almost all state-of-the-art techniques can provide good results only if particular conditions are satisfied; works in this research area very often also lacks of a serious scientific approach and of tests on real images, that is a necessary validation step.

Blur is a major problem affecting several technical areas, spacing from optical to photography, medicine and robotics. In all these fields, the development of an architecture able to receive blurry (and possibly noisy) input images and to return restored outcomes would represent a significant improvement. Moreover, if such architecture were also able to work in real-time (i.e., within a time so small that does not affect overall system performances), then it can be used as a standard pre-processing step in several applications and surely allow further applications obtaining better results. In fact, it is easier for each application that has to process images to work on sharp inputs, as details will be more clear and so the outcomes [1].

On the other hand, there are cases when no hardware support may be guaranteed, while timing requirements are very strict; in such cases, there is no the possibility of using complex and resources-consuming deblurring techniques. However, simple software arrangements may be used to handle blur, considering its effects while processing input images. The overall system performances

may highly increase also in this case. One example is described in [2].

## 2. Deblur and Hardware acceleration

The goal of our research work is to enhance performances of a generic image processing algorithm by developing a pre-processing deblurring architecture, enhanced by hardware acceleration, able to restore in real-time images of different sizes, independently from the severity of the blur affecting them. Such architecture only needs human interaction before its setup, when it is necessary to set expected blur parameters.

### Deblurring techniques

Existing deblurring algorithms produce outcomes whose quality strictly depends from the kind of images they are applied to. On the other hand, developing a totally new deblurring technique would require very deep mathematical knowledge. For this reason, we have focused on reshaping already known techniques, underlining weakness and strength points of each, to develop a preliminary system that can handle different blur effects and assuring in every case a good quality of the outcomes and high performances.

### Hardware acceleration

At the end of our research phase, we have developed a deblurring software that offers good performances and guarantees good quality outcomes. We have focused our efforts on optimizing the algorithm by splitting it into several sub-modules, which can be executed in pipeline by different processing units. These units have been described using VHDL and implemented on a reconfigurable FPGA, in order to achieve the highest degree of performance. Our preliminary analysis confirms that a deblurring algorithm may be effectively implemented on a modern FPGA board (from the Xilinx Virtex7 family) and used to deblur more than 30 VGA frames per second. This opens up new perspectives for imaging devices in real-life systems.

[1] G. Airò Farulla, "Design of a High Performance Core for Removing Blur Effect on Images", MsC Thesis, 2013.

[2] L. O. Russo, G. Airò Farulla, M. Indaco, S. Rosa, D. Rolfo, and B. Bona, "Blurring Prediction in Monocular SLAM," in International Design and Test Symposium, 2013. IDT 2013. IEEE International. IEEE, 2013, in press.