Call for Papers

Test and Reliability Track at DATE 2014

ICC, Dresden, Germany - March 24-28, 2014

The **Design, Automation and Test in Europe conference and exhibition** is the main European event bringing together designers and design automation users, researchers and vendors, as well as specialists in the hardware and software design, test and manufacturing of electronic circuits and systems.

One of the tracks of DATE is devoted to **Methods, Tools and Innovations for Testing and Reliability of Electronic Circuits and Systems**. You are invited to submit your research contributions to the test track. This five-day event consists of a **conference** with plenary keynotes, regular papers, interactive presentations, panels and hot-topic sessions, tutorials, master courses and workshops. The scientific conference is complemented by a commercial **exhibition** showing the state-of-the-art in design and test tools, methodologies, IP and design services. Both the conference and the exhibition, together with the many user group meetings, fringe meetings, university booth and social events offer a wide variety of opportunities to meet and exchange information.

TOPICS

T1 Defects, Faults, Variability and Reliability Analysis and Modeling

Chairs: Rob Aitken (ARM, US), Joan Figueras (Universitat Politècnica Catalunya, ES)

Identification, characterization and modeling of defects, faults and degradation mechanisms; defect-based fault analysis; reliability analysis and modeling, Failure mode and effect analysis (FMEA) and physics of failures; noise and uncertainty modeling; test and reliability issues in emerging technologies; modeling and mitigation of physical sources of errors such as process, voltage, temperature and aging variations; process yield modeling and enhancement.

T2 Test Generation, Simulation, Diagnosis and System Test

Chairs: Grzegorz Mrugalski (Mentor Graphics Poland, PL), Bernd Becker (University of Freiburg, DE)

Test pattern generation (TPG); fault simulation; high-level TPG; delay TPG; low-power TPG; TPG for memories and FPGAs; system test; diagnosis; debug; post-silicon validation; testing at various levels of a system: embedded core, System-on-Chip, System-in-Package, System-on-Package, Package on Package, board, system; testing 3D chips; Network-on-Chip test; hardware/software system test; processor based test; infrastructure IP.

T3 Test for Mixed-Signal, Analog, RF, MEMS/bioMEMS/MOEMS

Chairs: Haralampos Stratigopoulos (TIMA Laboratory, FR), Andre Ivanov (UBC, CA)

Test generation; test instrumentation; built-in test; built-in self-test; design-for test; defect characterization; failure analysis; fault modeling; fault simulation; defect-oriented test; test coverage metrics and estimation; adaptive test; self-healing/self-calibration/self-adaptation; design-for-manufacturability and design-for-yield; diagnosis and self-repair; test economics.

T4 Design-for-Test, Test Compression, Test Access

Chairs: Rohit Kapur (Synopsys, US), Paolo Prinetto (Politecnico di Torino, IT)

Design-for-test, -debug, and -manufacturability; built-in self-test and built-in diagnosis; synthesis for testability; test resource partitioning, embedded test; test data compression; scan-based test and diagnosis; BIST for memories and regular structures, low power DfT techniques, DfT for secure systems, DfT economics; industrial test: test equipment, including ATE hardware and software, probe stations, handlers; multi-site testing; economics of test; case studies.

T5 On-Line Test, Fault Tolerance and Reliable System Design

Chairs: Lorena Anghel (TIMA, FR), Fabrizio Lombardi (Northeastern University, US)

Transient fault evaluation; soft error susceptibility; on-line testing and fault tolerance for signal integrity; concurrent monitors and diagnosis; coding techniques; in-field testing and diagnosis; on-line testing; high availability systems; secure and safe circuits and systems design; dependability evaluation, reliable system design; redundant systems design; hardware/software recovery; self-repair; fault tolerance; on-line testing and fault tolerance for industrial applications.

PAPER SUBMISSION

All manuscripts must be submitted electronically before **Friday, September 13, 2013**, following the instructions on the conference Web page:

www.date-conference.com

The accepted file format is PDF. Any other format and manuscripts received in hard-copy form will not be processed.

Papers can be submitted for either formal oral presentation or for interactive presentation. Oral presentations require novel and complete research work supported by experimental results. Interactive presentations are expected to articulate emerging and future design, verification and test problems including work in progress and identify open problems that merit innovative future research. These presentations are given on a laptop in a face-to-face discussion area.

Submissions should not exceed 6 pages in length for oral-presentation papers and 4 pages in length for interactive-presentation papers, and should be formatted as close as possible to the final format: A4 or letter sheets, double column, single spaced, Times or equivalent font of minimum 10pt (templates are available on the DATE Web site for your convenience). To permit blind review, submissions should not include the author names. Any submission not in line with the above rules will be discarded.

All papers will be evaluated with regard to their suitability for the conference, originality, and technical soundness. The Programme Committee reserves the right to reorient oral-presentation papers to interactive-presentation and vice versa, to obtain the most suitable presentation format.

INFORMATION

Cecilia Metra - DATE Test and Reliability Track Chair

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