W2 Quo Vadis, Virtual Platforms? Challenges and Solutions for Today and Tomorrow

**W2 Quo Vadis, Virtual Platforms? Challenges and Solutions for Today and Tomorrow**

**Session Type:**
workshop

**Date:** Fri, 2012-03-16
**Time:** TBD
**Location / Room:** TBD

[http://qvvp12.offis.de](http://qvvp12.offis.de)

**Organisers**
- Rainer Leupers – RWTH Aachen University, DE
- Christian Haubelt – University of Rostock, DE
- Achim Rettberg – Carl von Ossietzky University Oldenburg, DE
- Kim Gruettner [Kim.Gruettner@offis.de](mailto:Kim.Gruettner@offis.de) – OFFIS – Institute for Information Technology, DE

**Description**

Nowadays, the deployment of Virtual Platform models is an industry-proven technique in a wide variety of design tasks from pre-silicon software development to performance analysis and exploration. With the increasing complexity, both in terms of the applications and the target platforms (e.g. increasing number of cores, more complex memory hierarchies), the Virtual Platform per se is not an answer to all of today’s design challenges. But by adding further abstraction to the models, an increasing need for automated mapping, refinement, and model transformations is needed. Formal, static, and dynamic analysis methods are increasingly dependent on platform details, requiring traceability during all design phases. This workshop aims to bring together developers, researchers, and managers from industry and academia to develop a perspective for the future use of Virtual Platforms by exchanging knowledge about current and future requirements and their possible solutions. The workshop will also provide some space for the provision of state of the art and tangible results and session on tool demos. Questions to be addressed during the workshop are:

- How to efficiently generate a Virtual Platform for new applications and HW platforms?
- How to close the implementation/refinement gap?
- Which properties of a real system can be captured?
- What are the requirements for future Virtual Platforms?
- How can Virtual Platforms support the development of future real-time applications for MPSoCs?

In this workshop, different points of view will be discussed by

- users of Virtual Platforms from different domains
- tool vendors already offering Virtual Platform tools and modeling techniques, and
- academic research institutes from around the world showing recent progress in Virtual Platform synthesis and core technologies.

**Workshop Format and Structure**

The workshop presentations will be by invitation, an open call will be issued for poster session presentations. Poster submissions for each topic area will be reviewed by the workshop organizers and the speakers respectively.

**Topic Areas**
The workshop will have three main sessions:

1. **System Synthesis – From System-Level Models to (Virtual) Platforms**
2. **Virtual Platforms Techniques – State of the Art and Beyond**
3. **Implementing Virtual Platforms on Multi-Application Multi-Core Platforms**

After each workshop session will be a combined 30-60 min coffee and poster break.

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**Program**

<table>
<thead>
<tr>
<th>Time</th>
<th>Session</th>
<th>Speaker/Institution</th>
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<tbody>
<tr>
<td>0845</td>
<td>Welcome and Introduction</td>
<td>Rainer Leupers – RWTH Aachen University, DE</td>
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| 0900  | **SESSION 1: System Synthesis – From System-Level Models to (Virtual) Platforms**  
On today’s Virtual Platforms, the communication is expressed at the transaction-level, usually on top of memory-mapped interconnect models. The mapping and refinement of system-level application models to such platforms is still a challenging task. Exploiting the properties of stricter models of computation (MoC) during this mapping requires knowledge of certain platform artifacts, which may or may not be fixed beforehand. | Rainer Dömer – University of California, Irvine, US      |
| 0930  | Recoding Embedded Applications into Flexible System-Level Models          | Jürgen Teich – University of Erlangen-Nuremberg, DE     |
| 1000  | **MPSoC Platforms for mobile devices: HW and SW development based on the Nucleus methodology**  
Torsten Kempf – RWTH Aachen University, DE | |
| 1030  | Poster Session & coffee break                                            | (list of posters see below)                             |
| 1100  | **SESSION 2: Virtual Platform Techniques – State of the Art and Beyond**  
With SystemC TLM-2.0, an industrial standard for modeling interoperable Virtual Platforms has been defined. Still, for the platform integration as well as for the analysis of functional and non-functional properties (like power, temperature, etc) different, mainly unconnected approaches exist. In this session, the industrial state-of-the-art for rich Virtual Platform models as well as recent research results and standardization activities are presented. | Yossi Veller – Mentor Graphics, IL                      |
| 1130  | Scalable Transaction Level Modeling Methodology for Function, Communication, Timing and Power  
Yossi Veller – Mentor Graphics, IL | |
<p>| 1200  | LUNCH BREAK                                                             |                                                        |</p>
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<thead>
<tr>
<th>Time</th>
<th>Title</th>
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<tbody>
<tr>
<td>1300</td>
<td>HW/SW Verification from an Open SystemC virtual prototype through simulation, emulation, and FPGA prototyping</td>
<td>Leonard Drucker – Cadence, US</td>
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<tr>
<td>1330</td>
<td>High-Level Synthesis, TLM Power State Machines, and advanced tracing for Virtual Platforms</td>
<td>Philipp A. Hartmann – OFFIS – Institute for Information Technology, DE</td>
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<td>SESSION 3: Implementing Virtual Platforms on Multi Application Multi-Core Platforms</td>
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<td>Mapping multiple concurrent applications to multi-core platforms under (hard) real-time constraints is a very challenging task. Multi-core WCET analysis strongly depends on platform details. To achieve composability and segregation of heterogeneous applications running on a single platform, even further (performance, power, etc.) virtualization may be needed. Dedicated platforms providing hardware support for analyzability may be the answer.</td>
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<tr>
<td>1400</td>
<td>Computation Architecture and Platform for Smart Grid Applications</td>
<td>Moritz Neukirchner – TU Braunschweig, DE</td>
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<tr>
<td>1430</td>
<td>Poster Session &amp; coffee break</td>
<td>(list of posters see below)</td>
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<tr>
<td>1500</td>
<td>CoMPSoC: A Composable and Predictable Execution Platform</td>
<td>Kees Goossens – Eindhoven University of Technology (TU/e), NL</td>
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<tr>
<td>1530</td>
<td>Cross-Domain Reference Architecture for Embedded Systems</td>
<td>Roman Obermaisser – University of Siegen, DE</td>
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<tr>
<td>1600</td>
<td>Closing Remarks</td>
<td>Christian Haubelt – University of Rostock, DE</td>
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<td>1615</td>
<td>CLOSE</td>
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**POSTERS:**

**Virtual Platform Generation Using TECS Software Component and SCE**
Takuya Azumi - Ritsumeikan University, JP
Yuko Hara-Azumi - Ritsumeikan University, JP
Rainer Dömer - University of California, Irvine, US

**Architecture Exploration of Multicore Systems-on-Chip using a TLM-based Framework**
Mona Safar - Ain Shams University, ET
Magdy El-Moursy - Mentor Graphics Corporation, ET
Mohamed Abdelsalam - Mentor Graphics Corporation, ET
Ashraf Salem - Technology Innovation and Entrepreneurship Center (TIEC), ET

**Virtual Platform for Mixed-Time Criticality Applications: The CoMPSoC Architecture and SDF3 Design Flow**
Benny Akesson - Eindhoven University of Technology, NL
Sander Stuijk - Eindhoven University of Technology, NL
Anca Molnos - Delft University of Technology, NL
Martijn Koedam - Eindhoven University of Technology, NL
Radu Stefan - Eindhoven University of Technology, NL
Andrew Nelson - Delft University of Technology, NL
Ashkan Beyranvand - Delft University of Technology, NL
Kees Goossens - Eindhoven University of Technology, NL

**Source-Level Timing Simulation of Embedded Software Considering Compiler Optimizations**
Efficient Analysis of SystemC Models
Simon Roth, BOSCH GmbH, DE
Wolfgang Rosenstiel - University of Tuebingen, DE

Virtual Platform for Embedded System Power Estimation
Santhosh Kumar Rethinagiri - INRIA Lille Nord Europe, Univ. of Valenciennes, FR
Rabie Benatitallah - UVHC/LAMIH, FR
Jean-Luc Dekeyser - Inria, FR

Domain Specific Virtual Platforms
Francisco Mendoza - FZI Forschungszentrum Informatik, DE
Juergen Becker - Karlsruhe Institute of Technology, DE

Dynamic Resource Management for Virtualized Mixed-Criticality Systems
Stefan Groesbrink - University of Paderborn, DE
Simon Oberthuer - University of Paderborn, DE
Daniel Baldin - University of Paderborn, DE

Quo Vadis, Virtual Platforms? A Posse ad Esse, hic Platforma Vitutis Est!

Scalable Multi-Core Virtualization for Embedded System-on-Chip Architectures
Alexander Biedermann - TU Darmstadt, DE
Sorin Huss - TU Darmstadt, DE

Poster Submission Instructions
Authors are invited to submit contributions as up to 2-page long abstracts. On-going works are welcome. All submissions must be written in English, and only PDF files are accepted. All 2-pages abstract must be prepared in accordance with the DATE manuscript style. All submitted 2-page abstracts should clearly identify the relevant session (System Synthesis, Virtual Platforms Techniques, or Implementing Virtual Platforms on Multi-Application Multi-Core Platforms) and will undergo the same review process (at least 2 reviews per contribution).

Important dates
- Deadline for 2-page abstract submission (extended): **November 04, 2011** November 30, 2011
- Notification of acceptance (extended): **December 02, 2011** December 23, 2011
- Final 2-page abstract and one page poster submission: **February 03, 2012**

Proceedings
A workshop digest based upon the 2-page abstract and one-page poster will be distributed to all participants of the workshop. In addition to the workshop digest, the organizers plan to invite selected speaker and poster presenters to submit original work to a Springer Book on “Virtual Platforms for MPSoC Design: Principles & Practice”.

Note that the posters presented at the DATE workshops are NOT disseminated through the official DATE proceedings or through any other formal channels, such as, for example, the IEEExplore or the ACM Digital Library.

Program Committee
Rainer Dömer (USA)
Leonard Drucker (USA)
Rolf Ernst (DE)
Kees Goossens (NL)
Kim Grütter (DE)
Philipp A. Hartmann (DE)
Christian Haubelt (DE)
Tim Kogel (DE)
Rainer Leupers (DE)
Adam Morawiec (FR)