G2 Testing TSV-Based 3D Stacked Ics

Three-dimensional stacking of multiple integrated circuits has benefits in terms of combining heterogeneous technologies and achieving a small footprint. The semiconductor industry is preparing itself to make a major step forward in three-dimensional stacking, now that the technology of TSVs is becoming available. TSVs are conducting nails which extend out of the back-side of a thinned-down die, enabling the vertical interconnect to another die. TSVs are high-density, low-capacitance interconnects compared to traditional wire-bonds, and hence allow for many more interconnections between stacked dies, while operating at higher speeds and consuming less power. TSV-based 3D technologies enable the creation of a new generation of ‘super chips’ by opening up new architectural opportunities. 3D-SICs combine a smaller form factor and lower overall manufacturing costs with many other compelling benefits, and hence their technology is quickly gaining ground.

Like all micro-electronic products, 3D-SICs need to be tested for manufacturing defects incurred during their many, high-precision, and hence defect-prone manufacturing steps. These tests should be both effective and cost-efficient. Solutions regarding test flow, test contents, and test access need to be developed before 3D-SICs can be brought to the market. Next to all basic and most advanced test technology issues, 3D-SICs have some unique new test challenges of their own. These challenges include (1) development of new fault models and corresponding tests for TSV-based interconnects and new 3D-induced intra-die defects, (2) wafer probing on small and numerous micro-bumps and/or TSV tips and pads under stringent damage requirements, (3) handling of and probing on wafers with thinned-die stacks, (4) the design, partitioning, and optimization of DfT architectures that span across multiple dies, and (5) optimization of the test flow for maximum effectiveness and lowest cost.

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SPEAKERS’ BIOGRAPHIES

Erik Jan Marinissen received the MSc degree in Computing Science and the PDEng degree in Software Technology from Eindhoven University of Technology in 1990 and 1992, respectively. He is currently a Principal Scientist at IMEC in Leuven, Belgium. Prior to IMEC, he was with NXP Semiconductors and Philips Research, both in Eindhoven, The Netherlands. Marinissen’s research interests include all topics in the domain of test and debug of integrated circuits. He is a co-author of more than 140 journal and conference papers and a co-inventor of nine granted US and EU patent families. He is a recipient of Best Paper Awards at the Chrysler-Delco-Ford Automotive Electronics Reliability Workshop in 1995, the IEEE International Board Test Workshop in 2002, and the Most Significant Paper Award at the IEEE International Test Conference in 2008. Marinissen served as an Editor-in-Chief of IEEE Std. 1500. He is the founder and chair of the IEEE Standardization Study Group on 3D-Testing. He serves on numerous conference committees, including IEEE Asian Test
Symposium (ATS), IEEE European Test Symposium (ETS), Design, Automation and Test in Europe (DATE), IEEE International Test Conference (ITC), and IEEE VLSI Test Symposium (VTS). He is a founder of workshops on 'Diagnostic Services in Network-on-Chips' (DSNOC), '3D Integration', and '3D-TEST'. Marinissen serves on the editorial boards of IEEE 'Design & Test of Computers', IET 'Computers and Digital Techniques' (IET-CDT), and Springer’s 'Journal of Electronic Testing: Theory and Applications' (JETTA). He is an IEEE Fellow and a Golden Core Member of Computer Society. Marinissen presented full-day tutorials on the topic of modular SOC testing and 3D-SIC testing at ATS, DATE, ETW, ITC, and VTS.

Yervant Zorian has served as Virage Logic's Vice President and Chief Scientist since joining the company in 2000. Prior to that, Dr. Zorian served as a Distinguished Member of the Technical Staff at Lucent Technologies, Bell Laboratories and Chief Technical Advisor to LogicVision. Dr. Zorian also serves as the Vice President of the IEEE Computer Society for Conferences and Tutorials and is the Editor-in-Chief Emeritus of IEEE Design & Test of Computers. He founded and presently chairs the IEEE 1500 standardization working group for embedded core test, and has authored over 250 papers and four books. Dr. Zorian has received a number of best paper awards, is an honorary doctor of the National Academy of Sciences of Armenia, is a Fellow of the IEEE, and is the recipient of the 2005 IEEE Industrial Pioneer Award. Dr. Zorian received an MSc degree from the University of Southern California, and a Ph.D. from McGill University.

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