One Step Autozeroing Two Stage Amplifier with Floating Gate Memory Cells

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Abstract

Precision operational amplifiers form a key building block in mixed signal systems. An autozeroing OpAmp using floating gate memory cells will be shown and measurement results will be presented.

1. Introduction

Precision operational amplifiers form a key building block in mixed signal systems. To achieve high precision, a reduction of the input offset voltage is crucial. This offset removal can be done with various mechanisms, including laser trimming, chopper stabilisation or autozeroing using an auxiliary amplifier in addition to the main amplifier path as developed in [1]. This requires large capacitors to store the calibration values. By reducing the size of the storage capacitors using floating gate memory cells, it is possible to design the amplifier including the autozeroing circuit on-wafer as a single-chip solution without additional external devices.

2. Autozeroing Amplifier

The general structure of an operational amplifier with a primary and an auxiliary path [1] can be seen in Fig. 1. The voltage gain of both paths can be described with $A = G_{m1}R$ and $A' = G_{m2}R$ respectively. $G_{m1}$ and $G_{m2}$ represent the differential pair of both paths while $R$ is a transimpedance amplifier.

![Figure 1: a) Autozeroing amplifier, b) timing diagram](image)

During clock phase $\Phi_0$ the storage capacitors $C_1$ and $C_2$ are discharged by the switches $S_0$. Then the voltage values are stored on both capacitors. For this purpose the switches $S_1$ are opened and $S_3$ and $S_4$ closed during clock period $\Phi_1$. During the transition from phase $\Phi_1$ to $\Phi_2$ (writing process to normal operation) a voltage error across the storage capacitors $C_1$ and $C_2$ is caused by the opening of switch $S_3$. The voltage across the capacitors during phase $\Phi_2$ can be described as

$$V'_C = V_C + \Delta V_C$$

The error voltages change the result of the storing process and need to be minimized to achieve low effective offset values.

The switches $S_0$ and $S_1$ in Fig. 1 are replaced by the circuit shown in Fig. 2. It features the storage capacitor $C_S$ and the ideal switches $S_0$ and $S_3$ which represent tunneling capacitors. Using the Fowler Nordheim tunneling effect [2], the node $F$ can be charged and discharged with tunneling currents [3], [4]. The tunneling capacitor acts like a switch that is open below a threshold voltage of about $\pm 5.5...6.5V$, above which a current starts to flow.

![Figure 2: a) Simple switch, b) sample and static hold block](image)

As the starting value of the floating node $F$ is unknown, the structure is erased first by applying a high negative programming voltage to node $V_{PN}$. Then the supply voltage of the amplifier is switched from $V_{DD}$ to $V_{PP}$, the high positive programming voltage and $V_{PN}$ is connected to GND. The positive input of the amplifier is connected to the reference voltage $V_{ref}$ and this value is stored on the floating node $F$. After the write process, the supply voltage of the amplifier is switched back to $V_{DD}$. The positive input is connected to $V_{DD}$ as well. During the read mode, the voltage at the internal node $F$ is sensed by a sense amplifier that is not shown in Fig. 2.
However, the switching of the supply voltage from $V_{pp}$ to $V_{DD}$ causes a voltage error on the internal node F. This error voltage is 

$$
\Delta V_C = V_{fw} - V_{fr}
$$

As the charge on the floating node F is constant the amount of charge can be described as 

$$-C_{iw}(V_{out,w} - V_{fp}) + C_S V_{fp} = -C_{iw}(V_{DD} - V_{fr}) + C_S V_{fr}
$$

Therefore, the error voltage $\Delta V_C$ can be described with $C_T = C_{iw} + C_S$ as 

$$
\Delta V_C = C_{iw}/C_T (V_{out,w} - V_{DD})
$$

and can be minimized by increasing the size of the storage capacitor $C_S$ or by reducing the voltage difference $V_{out,w} - V_{DD}$, i.e. connecting the supply voltage pin of the amplifier to the highest available voltage without starting tunneling currents to flow.

3. Measurement results

Two types of the two stage operational amplifier were fabricated using a 0.35$\mu$m double well CMOS process with an EEPROM module. Both, Type A autozeroing and Type B control devices, are shown in Fig. 3.

The OpAmp has an open loop gain of more than 120dB and is stable for a capacitive load up to $C_L=380pF$. Fig. 4 shows the offset voltage over the whole common mode input voltage range before and after calibration. There are two offset ranges mirroring the PMOS and NMOS differential pairs between which the offset voltage changes significantly. Only the PMOS input stage was calibrated. The offset voltage values before calibration varied between $-8mV$ and $8mV$ as it is defined by the voltages on the capacitors $C_1$ and $C_2$ and thereby showed the complete offset calibration range. After recalibration, the offset range was $-100...100\mu V$. The endurance of the devices was tested by repeating a cycle of erase-read-write-read operations. Degradation was found beyond a number of 10,000 cycles which equals about 27 years of recalibration once a day. Data retention tests showed that the calibration values remain constant over several months for devices that already experienced up to 1,000 programming cycles.

![Figure 3: Chip photograph](image)

![Figure 4: Offset voltage before and after calibration](image)

4. Conclusion

A novel two stage amplifier using an autozeroing based on floating gate memory cells instead of external capacitances or laser trimming was presented, that is suitable for applications requiring recalibration at power on. Measurement results show an offset reduction to a value of $\pm 100\mu V$. Endurance measurement results have proven that the OpAmp is suitable as a precision amplifier used in applications that require a recalibration at power on.

5. References


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