Call for Participation

DATE 2009 Friday Workshop on

3D Integration

— Technology, Architecture, Design, Automation, and Test —

Palais des Congrès Acropolis — Nice, France
Friday April 24, 2009
http://www.date-conference.com/conference/date09-workshop-W5

The **Design, Automation, and Test in Europe** conference and exhibition is the main European event bringing together designers and design automation users, researchers and vendors, as well as specialists in hardware and software design, test and manufacturing of electronic circuits and systems. The conference includes plenary invited papers, regular papers, panels, hot-topic sessions, tutorials and workshops, two special focus days, and a track for executives. **Friday Workshops** are focusing on emerging research and application topics. At DATE 2009, one of the Friday Workshops is devoted to **3D Integration**. This one-day event consists of a plenary keynote, regular and poster presentations, and a panel session.

WORKSHOP DESCRIPTION

3D Integration is a promising technology for extending Moore's momentum in the next decennium, offering higher transistor density, faster interconnects, heterogeneous technology integration, and potentially lower cost and time-to-market. But before 3D chips can be produced, new capabilities are needed: process technology, architectures, design methods and tools, and manufacturing test solutions. The goal of this Workshop is to bring together researchers, practitioners, and others interested in this exciting and rapidly evolving field, in order to update each other on the latest state-of-the-art, exchange ideas, and discuss future challenges.

WORKSHOP PROGRAM

The workshop program contains the following elements.

- A keynote address: "The Promise of Through-Silicon Vias" by Sitaram Arkalgud (Sematech, US)
- An invited talk: "Requirements for Design-for-3D Environment" by Riko Radojcic (Qualcomm, US)
- Two sessions with in total six regular presentations
- Two poster sessions
- A panel session discussing "The Future of 3D Integration from All Angles"

For the detailed version of the program, please turn over.

PARTICIPATION and REGISTRATION

You are invited to participate in the workshop. Participation requires registration and a registration fee. Registration will be available through the DATE'09 web site, as well as on-site in Nice, France. Check the DATE web site (http://www.date-conference.com) for rates and other information. Workshop registration includes luncheon, coffee breaks, and download access to the Electronic Workshop Digest, containing extended abstracts, papers, slides, posters.

MORE INFORMATION http://www.date-conference.com/conference/date09-workshop-W5

Erik Jan Marinissen – *General Chair*
IMEC
Smart Systems and Energy Technology
Kapeldreef 75
3001 Leuven, Belgium
E-mail: erik.jan.marinissen@imec.be

Yann Guillou – *Program Co-Chair*
ST-Ericsson
Wireless Multimedia Division
12, rue Jules Horowitz – BP 217
38019 Grenoble cedex, France
E-mail: yann.guillou@stericsson.com

Geert Van der Plas – *Program Co-Chair*
IMEC
Smart Systems and Energy Technology
Kapeldreef 75
3001 Leuven, Belgium
E-mail: geert.vanderplas@imec.be

08:30h: SESSION 1: OPENING

Moderator: Lisa McIlrath – R3Logic, US

08:30h: Welcome Address

08:45h: Keynote Address: The Promise of Through-Silicon Vias

Sitaram Arkalgud – Sematech, US

The twin drivers of all advances in the semiconductor industry have been ever increasing performance and productivity. With tremendous strides in lithography and device development over the last several decades, achieving both has been possible. However, with fundamental issues and cost concerns surrounding new technology elements at 32nm and below, the viability of traditional lithography and device scaling to stay on the productivity curve becomes questionable. One of the technologies gaining popularity has been Through-Silicon Vias (TSVs) for stacking chips in the third dimension. This presentation will discuss the merits of 3D TSVs, state of the art on 3D, the risks and challenges involved, the timeline, the need for understanding the cost implications and manufacturability, and the necessity for standardization and classification.

09:30h: Invited Talk: Requirements for Design-for-3D Environment

Riko Radojcic – Qualcomm, US

Qualcomm's roadmap for 3D technology is outlined, and the corresponding requirements for a holistic design environment necessary to define and implement optimized 3D products are described. The focus is on the design environment and EDA tools necessary for 'Stage 1' class of products, consisting of a functionally partitioned two-die stack. The design environment requirements are segregated into three classes of methodologies and the associated EDA technologies.
(a) "TechTuning" technologies required to co-optimize process technology and chip design requirements, and to define and validate the design rules and models required for 3D Design Authoring,
(b) "PathFinding" technologies required to co-optimize system and technology specifications, and to define the optimum architecture for the 3D process and design, and to generate the constraints required for Design Authoring, and
(c) "Design Authoring" flow and the EDA technology upgrades required to implement chip design for 3D stacks.
The status of the collaborative efforts, supported by Qualcomm and a set of partners, to develop and evaluate each of these technologies is summarized. Key results and challenges will be presented.

10:00h: POSTER SESSION 1

22 posters (see right) - coffee + tea break

10:30h: SESSION 2

Moderator: Peter Schneider – Fraunhofer Institute, DE

10:30h: 3D Integration Perspective for Multimedia Products
Dominique Henoff, Laurent Bonnot – ST Microelectronics, FR

11:00h: Z-Axis Interconnections: Fabrication and Electrical Performance
Voya R. Markovich, Rabindra N. Das, Michael Rowlands, John Lauffer – Endicott Interconnect Technologies, US

11:30h: Impact of Design Choices on 3D SiC Manufacturing Cost
Dimitrios Velenis, Michele Stucchi, Erik Jan Marinissen, Eric Beyne – IMEC, BE

12:00h: LUNCHEON BREAK

13:00h: SESSION 3

Moderator: Yuan Xie – Pennsylvania State University, US

13:00h: Clock and Power Distribution Networks for 3D Integrated Circuits
Ioannis Savidis, Eby G. Friedman – University of Rochester, US; Vasilis F. Pavlidis, Giovanni De Micheli – LSI-EPFL, CH

13:30h: Hierarchical Cache System for 3D-Multi-Core Processors in Sub 90nm CMOS
Kumiko Nomura, Keiko Abe, Shinobu Fujita, Yasuhiko Kurosawa, Atsushi Kageshima – Toshiba Corp., JP

14:00h: Test Strategies for 3D Die-Stacked Integrated Circuits
Dean L. Lewis, Hsien-Hsin S. Lee – Georgia Institute of Technology, US

14:30h: POSTER SESSION 2

22 posters (see right) - coffee + tea break

15:00h: PANEL SESSION

"The Future of 3D Integration From All Angles"

Moderator: Peter Ramm – Fraunhofer Institute, DE

Panelists: Roger Carpenter – Javelin Design Automation, US
Krishnendu Chakrabarty – Duke University, US
Paul Siblerud – Semitool, US
Nicolas Sillon – CEA-LETI, FR
Pascal Urard – ST Microelectronics, FR
Geert Van der Plas – IMEC, BE

16:00h: CLOSURE

POSTER SESSIONS 1 and 2

1. 3D Technologies and Data Structures – An Overview,
Robert Fischbach, Jens Lienig – Dresden University of Technology, DE
2. System-Level Exploration of 3D Interconnection Schemes,
Kostas Siozios, A. Papanikolaou, Alexandros Bartzas, Dimitrios Soudris – National Technical University of Athens, GR
3. 3D Integrated Smart Antenna Systems,
Nakul Haridas, Tughrul Arslan – University of Edinburgh, UK
4. 3D Integration Program Overview,
Laurent Bonnot, Pascal Ancey, Damien Riquet, Pascal Urard – ST Microelectronics, FR; David Henry, Astrid Astier – CEA Léti, FR
5. Topology Exploration and Buffer Sizing for 3D Networks-on-Chip,
Alexandros Bartzas, Kostas Siozios, Dimitrios Soudris – National Technical University of Athens, GR
6. Closed-Form Equations for Through-Silicon Via Parasitics in 3D ICs,
Roshan Weerasekera, Dinesh Pamunuwa, Matt Grange – Lancaster University, UK; Hannu Tenhunen, Li-Rong Zheng – KTH, SE
7. 3D-NOCs, TSVs, Asynchronous Circuits, and Serial Vertical Links,
A. Sheibanyrad, F. Pétrot – TIMA/SLS, FR
8. Modular Modeling of RF Behavior of Interconnect Structures in 3D Integration,
Jörn Stolle, Sven Reitz, Peter Schneider, Andreas Wilde – Fraunhofer Institute for Integrated Circuits, DE
9. Evaluating Noise Coupling Issues in Mixed-Signal 3D ICs,
Liuchun Cai, Ramesh Harjani – University of Minnesota, US
10. Design, Verification and Simulation of 3D Circuit,
Guruprasad Katti, Bart De Wachter, Marc Nelis, Morin Dehan, Miroslav Cupak, Kris Croes, Gerd Beeckman, Pol Marchal, Michele Stucchi – IMEC, BE; Wim Dehaene – Katholieke Universiteit Leuven, BE
11. Examination of Delay and Signal Integrity Metrics in TSVs,
Matt Grange, Roshan Weerasekera, Dinesh Pamunuwa – Lancaster University, UK; Hannu Tenhunen – KTH, SE
12. On-Chip Waveform Capturing Functionality Partitioned for 3D Realization,
Yuuki Araga, Yoji Bando, Takushi Hashida, Makoto Nagata – Kobe University, JP
13. Thermal Aware Test Scheduling for Stacked Multi-Chip Modules,
Vinay N.S., Virendra Singh – Indian Institute of Science, IN; Erik Larsson – Linköping University, SE
14. A Prospective Analysis of High-Frequency Cross-Coupling Mechanisms for the Next 3D Packaging Generation,
Roberto Antonicelli – ST-Ericsson, BE
15. Power Integrity Issues in 3D ICs using TSVs,
Waqar Ahamd, Qiang Chen, Roshan Weerasekera, Hannu Tenhunen, Lirong Zheng – KTH, SE
16. Core Test Wrapper Optimization for 3D ICs with TSVs,
Brandon Noia, Krishnendu Chakrabarty – Duke University, US
17. Application of Substrate Noise Simulation Methodology to 3D Stacking,
S. Bronckers, Geert Van der Plas, Pol Marchal – IMEC, BE; Y. Rolain – Vrije Universiteit Brussel, BE
18. Impact of Thinning on 65nm Device Performance,
Dan Perry, Urmi Ray, Sam Gu, Mark Nakamoto, Wing Sy – Qualcomm, US; Kevin Wang – UC Berkeley, US; Wouter Ruythooren, Bart Swinnen, Yu Yang – IMEC, BE; Jurgen Burggraf, David Matheis-Weiss – EVGroup, AU; C.J. Berry, KiWook Lee – Amkor, US
19. Bandwidth Optimization for Through Silicon Via Bundles in 3D ICs,
Awet Yemane Weldezion, Li-Rong Zheng, Hannu Tenhunen – KTH, SE; Roshan Weerasekera, Dinesh Pamanuwa – Lancaster University, UK
20. Wafer-Level Based Manufacturing Technologies for Realization of TSV and 3D-Based Applications,
Stefan Pargfrieder, Daniel Burgstaller, Otto Bobenstetter, Bioh Kim – EV Group, AU
21. SOC Test Architecture and Method for 3D-IC,
Chih-Yen Lo, Yu-Tsao Hsing, Li-Ming Denq, Cheng-Wen Wu – National Tsing Hua University, TW
22. Vertical Links for 3D Network-on-Chip,
Igor Loi, Federico Angiolini, Luca Benini – Università di Bologna, IT