A High-Voltage Low-Power DC-DC buck regulator for automotive applications

G. Pasetti, L. Fanucci
Dept. of Information Engineering, University of Pisa
Pisa, Italy
giuseppe.pasetti@iet.unipi.it

R. Serventi
Austriamicrosystems AG
Navacchio (PI), Italy
www.austriamicrosystems.com

Abstract—This work presents a High-Voltage Low-Power CMOS DC-DC buck regulator for automotive applications. The overall system, including the high and low voltage analog devices, the power MOS and the low voltage digital devices, was realized in the Austriamicrosystems 0.35 HVCMOS technology, resulting in a 6.5 mm² die. The regulator is able to manage a supply voltage down to 4.5 V and up to 50 V and generates a fixed regulated output voltage of 5 V or a variable one in the whole automotive temperature range. The regulator sinks only a maximum of 1.8 μA of current in standby mode and a maximum of 25 μA when no load is connected. It can be used to supply low voltage devices from the battery when low power dissipation and low current consumption is needed. The system output current can be selected in the range 350-700 mA. When a higher output current is needed, it is possible to connect more regulators in parallel multiplying the output current without any problem.

Keywords: DC-DC regulator; buck converter; pulse frequency modulation; current control; low quiescent current.

I. INTRODUCTION

DC-DC regulators are used in modern cars to supply electronic systems from the battery voltage. These regulators have the task to stabilize the voltage to a fixed value, normally lower than the battery voltage, and filter the interferences coming from other systems through the battery cable. Indeed, in a car there are many different types of equipment all connected together with the battery.

The challenge for the regulators in automotive systems is to combine the harshest requirements, like 50 V input voltage capability, with low power consumption in standby mode and a low cost CMOS technology. The battery voltage in a car changes from 5 V during cranking to 50 V when the battery is temporarily disconnected (load dump) or one inductive load is disconnected. Low power consumption in standby mode is necessary in order to increase the lifetime of the battery when the car is stopped.

In this paper we present a new DC-DC regulator able to withstand all the automotive requirements, like 50 V as input voltage and 125°C as maximum ambient temperature, with very low current consumption both in standby mode and without load. The regulator can supply a current up to 700 mA, but, if a higher current is needed, it is possible to connect two or more regulators in parallel multiplying the output current without any problem. The regulator was designed in low cost 0.35μm HVCMOS technology from Austriamicrosystems AG.

II. DC-DC REGULATORS IN AUTOMOTIVE SYSTEMS

DC-DC regulators are systems that can convert a DC voltage to another DC voltage [1]. Compared to linear regulators, DC-DC regulators can achieve better performance in terms of power dissipation, output voltage capability and current capability, but they suffer in terms of output noise, line regulation and load regulation. DC-DC regulators ideally can have an efficiency of 100% and practical designs demonstrate efficiency of about 80-90% [2]. This performance can be achieved forcing the power MOS working as a switch and not as a resistor. Using this trick the power dissipated by the regulator is very low. This means that the efficiency goes up and normally no heatsink is needed thus reducing the system complexity. The linear regulators are very inefficient but compared to DC-DC regulators allow to obtain a better output performance: absence of any ripple and faster response to input and output variations; no electromagnetic interference (EMI) noise is generated. Indeed, in modern supply systems a linear regulator is used together with a DC-DC switching regulator, joining the high output performance of the former with the high efficiency of the latter.

In particular, designing automotive systems require paying attention in noise reject and in power dissipation. The regulator is one of the most stressed devices in terms of input noise. It is connected directly to the battery and the alternator and, for this reason, it has to withstand at the stress generated by them and by other electronic systems on a car. Furthermore automotive systems have to withstand at very wide ambient temperature range, from -40°C to 125°C.

In literature, it is possible to find two main branches of control techniques in DC-DC regulators: the voltage feedback control technique and the current feedback control technique. The voltage feedback is shown in figure 1 and it can be applied both with Pulse-Width-Modulation (PWM) and Pulse-Frequency-Modulation (PFM) techniques. It permits for a better load regulation, a lower ripple and to easily filter the EMI. Furthermore this control technique simplifies the design of the control loop, because no compensation is needed to
guarantee stability [3]. The current feedback is shown in figure 2 and, applied to PFM technique, it allows a better efficiency when low output current is needed, a limited maximum output current in the switch, a lower current consumption and a feed forward path that speeds up the regulation loop. This technique permits also to connect more than one regulator in parallel when a higher output current is needed [4-5]. So, given the target application of the regulator, a current control with a PFM technique is considered to be the most appropriate.

Figure 1. Voltage feedback technique

III. PROPOSED SOLUTION

The proposed solution is a DC-DC buck converter with a very low power consumption which is able to work in all typical automotive scenarios. The supply voltage can be in the range of 4.5 V - 50 V and the output voltage can be in the range of 1.25 V - V_supply. The system has two digital logic input pins that can be driven from any logical family supplied from 3.3 V to 50 V. If the first input is zero, the system goes into standby mode characterized by a very low current consumption. The second input can select the value of the maximum output current (I_max) between 700 mA or 350 mA. This possibility allows reducing the ripple voltage V_ripple by four, as explained in (1), when a low output current is needed.

\[ V_{\text{ripple}} = I_{\text{max}}^2 \frac{L_1}{2C_{\text{out}}} \frac{V_{\text{in}} - V_{\text{gt}}}{(V_{\text{in}} - V_{\text{out}})(V_{\text{out}} + V_{\text{gt}})} \]  

(1)

A simplified block diagram of the proposed regulator is shown in figure 3. The system can be divided into 4 main blocks: the internal power management unit; the control loop; the feedback path and the power stage.

A. Power Management Unit

The PMU is composed by a linear regulator, used to generate the internal supply voltages, a band-gap, used to generate the internal reference voltages and currents, a power-on-reset, that generates a reset signal when the supply falls down and removes it when the supply rises up, and an over-temperature sensor, used to turn off the entire system in case a high temperature is reached.

B. Control loop

As mentioned above, PFM is the best control technique for the target application. This kind of control allows for a better efficiency, when the output current is low, with respect to the PWM control strategy. Moreover, no oscillator is needed, thus speeding up the startup sequence and reducing the power consumption of the entire system. The use of PFM technique together with current sensing [6-7] provides the possibility to connect in parallel many devices thus increasing the maximum output power, when needed. This control is implemented using a SR-latch: setting it when the output voltage goes below the threshold and resetting it when the maximum current is reached. Furthermore the latch is reset when the maximum temperature is reached.

C. Feedback path

This chip is conceived to have an output voltage of 5 V or a variable output voltage selected by an external divider. The feedback selector senses the presence of an external divider and in such a case set the feedback path to use it, otherwise it set the feedback path to use the internal reference, carrying the output voltage at 5 V. The feedback path provides also the possibility to easily change the fixed output voltage \( V_{\text{out}} \) according to (2), where X can assume any integer from 1 and 132, by modifying just one metal.

\[ V_{\text{out}} = 1.25 \frac{132 \times X}{X} \]  

(2)

D. Power stage

The power stage is the most important block of the chip. It is made by a power-PMOS and a driver. The power-PMOS
was designed to have a low $R_{on}$, around 200 mΩ, and to withstand at currents up to 2 A. To lower production costs, as Power-PMOS we have used a standard HV-CMOS device, no further process steps are needed to make it. The driver is one of the most critical blocks for proper working of the regulator. It has to charge and discharge quickly the gate of power-PMOS, a capacitance of about 100 pF, to avoid waste of energy during transitions. The driver works in four different phases: a fast startup phase, a maintenance phase, a fast shutdown phase and a stand-by phase. During the first phase, the gate is charged with a constant current and the gate voltage falls down linearly. During the maintenance phase, the gate is biased with a constant voltage, maintaining constant the gate voltage and the ON resistance. During the fast shutdown phase, the gate is discharged with a constant current, the gate voltage rises up with the same slope of the startup phase to guarantee equal start and stop time. During the stand-by phase the gate and the source are connected together, shutting down the PMOS. These 4 phases and relevant transitions are showed in figure 4.

![Figure 4. Gate driver phases](image)

IV. SIMULATIONS AND LAYOUT

The entire system was simulated first to verify the functionalities and then to estimate the performance. As a first result the shutdown current consumption was simulated to be 1 μA as typical value and 1.8 μA as maximum value. The current consumption when no load is connected results in 15 μA as typical value and 25 μA as maximum value. Fig. 5 shows regulator waveforms in normal operation when the output current changes from 0 to 1 A. The first row is the output current, the second is the current flowing into the inductor, the third is the output voltage and the fourth is the voltage on the LX node (see Fig. 3).

A simulation with five modules in parallel was performed in order to prove the modularity and flexibility of the proposed regulator architecture. A maximum output current of 4.2 A was achieved and, for testing purpose, a fast transient from 0 to 4 A was simulated. The output capacity in this scenario was only 22 μF and this is the cause of the observed high ripple voltage. The output voltage (green line), output current (blue), voltage on two central nodes (2nd row) and current flowing in two inductors (3rd row) are shown in figure 6.

As far as simulated performance is concerned, Fig. 7 and 8 shows the output voltage versus the input voltage (in the range 5-50 V) with different inductors (10 μH and 39 μH) and for different output currents (100 mA and 500 mA).

![Figure 5. Normal mode waveform](image)

![Figure 6. Simulation of five modules](image)

![Figure 7. Line regulation with 100 mA and two different inductor](image)

![Figure 8. Line regulation with 500 mA and two different inductor](image)
The growth of the output voltage when the input voltage is in the range 40-50 V is due to the low inductance values. Equation (3) permits to calculate the minimum value of inductance $L_{\text{min}}$ starting from the desired output voltage $V_{\text{out}}$, the input voltage $V_{\text{in}}$ and some system parameters ($T_{\text{min}}$ and $I_{\text{max}}$). In this device the values of $T_{\text{min}}$ and $I_{\text{max}}$ are 600 ns and 1.4 A, respectively providing a value of $L_{\text{min}}$ of nearly 20 μH the minimum inductor is calculated in (4).

$$L_{\text{min}} = T_{\text{min}} \left(\frac{V_{\text{in}} - V_{\text{out}}}{I_{\text{max}}}\right)$$ (3)

$$L_{\text{min}} = 0.6 \times 10^{-6} \frac{50 - 5}{1.4} = 20 \mu\text{H}$$ (4)

Fig. 9 and 10 shows the load regulation performance in two practical cases: in Fig. 9 the supply voltage is 5 V and the regulator goes in dropout mode, keeping always ON the PMOS; in Fig. 10 the supply voltage is 12 V in the typical operating condition.

![Load Regulation 5V](image)

Figure 9. Load regulation with 5 V as supply voltage

![Load Regulation 12V](image)

Figure 10. Load regulation with 12 V as supply voltage

Figure 11 shows the layout of the entire chip. The Power-PMOS is placed on the right side, and the other blocks are placed on the left side. Between the left and the right side a large isolation is placed, avoiding substrate injection from the PMOS to low power devices. The placement was done considering the possibility to use the regulator as standalone or as a module in a larger electronic system. Indeed, all the required electronic blocks are placed together in the center of the chip. The electronic parts, as the PMU, that can be shared when the system is used as a module, are placed on the periphery. In this way it is easy to integrate this module in a larger system.

V. Conclusions

In this paper we proposed a DC-DC regulator designed in 0.35 μm HVCMOS technology from Austriamicrosystems. It has a very wide input voltage range, from 4.5 V to 50 V, and it sinks a very low quiescent current in standby (1.8 μA) and when no load is connected (25 μA). These features combined with the wide working temperature range, from -40°C to 125°C, allow using the regulator in automotive applications. Moreover, the proposed architecture allows for connecting more regulators in parallel in order to obtain a higher output current.

REFERENCES


