Abstract—Negative Bias Temperature Instability (NBTI) has become an important reliability concern for nano-scaled Complementary Metal Oxide Semiconductor (CMOS) devices. In this paper, we present an analysis of temperature impact on various sub-processes that contribute to NBTI degradation. We demonstrate our analysis on 90nm industrial design operating in temperature range 25-125°C. The key temperature impacts observed in our simulation are: (a) the threshold voltage increase in P-type Metal Oxide Semiconductor (PMOS) due to NBTI is very sensitive to temperature, and increases by 34% due to the temperature increment, (b) the hole mobility in PMOS inversion layer reduces by 11% with the temperature increment, and (c) the temperature has a marginal impact on the transistor delay, that increases by 3% with the temperature increment.

I. INTRODUCTION

The relentless scaling of CMOS devices has fronted reliability concerns [1]. Industrial data reveal that as oxide thickness reached to 4nm, NBTI became a dominant concern in CMOS devices [2]. NBTI degrades a PMOS transistor under negative gate stress at temperature (100-200°C). The aftereffects of NBTI on PMOS transistor include: (a) threshold voltage increase, (b) drain current degradation, and (c) speed degradation [2], [3]. Experimental results show that the aftereffects increase with rise in temperature [2].

To date the focus of NBTI literature is to model NBTI degradation under continuous and dynamic stress conditions at constant transistor temperature [3], [4], [5], [6]. However, transistors on a chip die experience significant temperature variation depending on their locations on chip and operation (stress/relaxation) conditions. Temperature variation due to operation condition is more significant. For example, Fig. 1 shows that variation may reach up to 50°K in DRAM at high end microprocessors [7]. Experimental results show that temperature variation reduces NBTI defined lifetime of an inverter by 2.2× for every 10°C increase in temperature [8]. Due to such a strong influence it is essential to consider impact of temperature on the sub-processes and in turn on the NBTI modeling for transistor accurate lifetime prediction.

In this paper, we present a calibrated analysis of NBTI sub-processes under temperature variation. The analysis enables NBTI modeling to accommodate temperature variation. The rest of the paper is organized as follows, Section II describes an NBTI model under dynamic stress conditions at constant temperature. Section III presents temperature impact on NBTI sub-processes. Section IV shows the simulation results and analysis. Finally Section V concludes the paper.

II. PREVIOUS NBTI MODEL

NBTI degradation has been modeled using Reaction Diffusion (RD) model [5]. Original model [5] suggested that PMOS degradation due to NBTI follows power law time dependence of $t^{1/4}$, e.g. for threshold voltage increase, $\Delta V_{th} \sim t^{1/4}$. Later refinements of the model [2], [6] assumed that the degradation follows, $t^{1/6}$. A recently proposed model [4], suggested that initially the degradation exhibit a $t^{1/4}$ dependence. As the time goes on, the degradation follow $t^{1/6}$ dependence. The models predict different behaviors between stress and recovery phases. We will describe both phases in the following discussion.

A. Stress Phase

NBTI degradations of PMOS transistor originate from Silicon Hydrogen bond (≡Si-H) breaking at Silicon-Silicon dioxide (Si-SiO₂) interface under negative gate stress ($V_{gs} = -V_{dd}$), as shown in Fig. 2(a). The figure shows that the broken Silicon bonds (≡Si-) act as interface traps, while the released Hydrogen (H) species diffuse towards poly gate. The interface traps count ($N_{IT}$) depend on ≡Si-H bond breaking rate ($k_f$), and ≡Si- bond recovery rate ($k_r$) at Si-SiO₂ interface [3]. The dependency can be written as:

$$\frac{dN_{IT}}{dt} = k_f(N_o - N_{IT}) - k_r N_{IT} N_H^0,$$

where $N_o$ and $N_H^0$ are initial bond density and Hydrogen density at the Si-SiO₂ interface. The H atoms released will: (a) diffuse toward the gate, (b) combine with other H atoms to produce H₂, or (c) recover the ≡Si- broken bonds. Similarly, H₂ will either diffuse towards poly gate, or dissociate to produce H atoms for ≡Si- bond recovery. The processes are schematically shown in Fig. 2(a), and formulated as [6]:

$$\frac{dN_H}{dt} = D_H \frac{d^2N_H}{dx^2} - k_H N_H^2 + k_{H2} N_{H2},$$

(2)

$$\frac{dN_{H2}}{dt} = D_{H2} \frac{d^2N_{H2}}{dx^2} + \frac{1}{2} k_H N_H^2 - k_{H2} N_{H2},$$

(3)
These sub-processes have distinct activation requirement, that interface traps generation consist of several sub-processes. During the second stage, the bond breaking domination continues to produce H atoms. The H atoms either participate in broken bonds recovery or interact with H atoms to produce H₂ molecules. However, due to lower H and H₂ densities, the diffusion sub-processes are negligible. Therefore, after rearranging Eq. 1 and Eq.2, the N_{IT} is given by [6]:

\[ N_{IT}(t) = \left( \frac{k_fN_0}{k_r} \right)^{2/3}(k_{HT})^{1/3}. \]  (4)

The third stage is very short. In this stage =Si-H bond breaking, H diffusion, and broken bond recovery sub-processes dominate the N_{IT} generation. The H₂ diffusion and dissociation sub-processes are still negligible [4] and N_{IT} is given by solving Eq. 1 and Eq. 2 as following:

\[ N_{IT}(t) = \left( \frac{k_fN_0}{k_r} \right)^{1/2}(D_Ht)^{1/4}. \]  (5)

During the last stage, most of the H atoms are converted to H₂, so activities of H₂ determine N_{IT} generation. The H₂ diffuse in SiO₂ layer, and dissociate to produce H atoms for =Si- bond recovery. Under such condition the N_{IT} generated are obtained by solving Eq. 1 and Eq. 3:

\[ N_{IT}(t) = \left( \frac{k_fN_0}{k_r} \right)^{2/3}(k_{HT})^{1/3}(6D_Ht^2)^{1/6}. \]  (6)

The model solutions given in [Eq. 4-6] show that the interface traps generation consist of several sub-processes. These sub-processes have distinct activation requirement, that causes time exponent variation for shorter and longer stress time.

### B. Recovery Phase

RD model also predicts that during recovery phase (\(N_{Ds} = N_{IT}(t)\)), H species diffuse toward the interface and recover the =Si- broken bonds. The recovered interface traps N\(_{IT}(t)\) can be written as [3]:

\[ N_{IT}(t) = 1/2N_{IT}(\xi,D_{H2}(t))^{1/α} \]  (7)

where \(ξ\) is the diffusion constant in oxide layer during recovery phase and \(N_{IT}\) is the number of H atoms that recover =Si-bonds. The interface traps N\(_{IT}\) survived during the recovery phase depends on the interface traps of the previous phase [say N\(_{IT}(t_o)\)] and recovered interface traps N\(_{IT}(t)\) [11]. Thus N\(_{IT}\) count survived during the recovery phase is given by:

\[ N_{IT}(t) = N_{IT}(t_o) - N_{IT}(t). \]  (8)

The Eq. shows that due to =Si- broken bond recovery in the recovery phase, the N\(_{IT}\) generated during dynamic stress are lower than continuous stress.

### III. NBTI MODEL WITH TEMPERATURE VARIATION

RD model assumes that NBTI degradation is temperature dependent, but does not give any physical basis for such dependency [6]. Therefore, impact of temperature on sub-processes contributing to interface traps generation must be properly understood. The understanding will enable accurate NBTI modeling and device lifetime prediction. In the following subsections we analyze temperature impact on NBTI sub-processes and on the interface traps count.

#### A. Temperature Impact during Stress Phase

RD model assumes that inversion layer holes are responsible for the breaking of =Si-H bond at Si-SiO₂ interface. Analysis reveals that during stress phase about 0.2-0.3eV energy is consumed to bring a hole close to =Si-H bond. The interaction results in breaking of =Si-H bond, producing an N\(_{IT}\) and H atom with 1.3eV energy release. Therefore, the net energy gain due to a single N\(_{IT}\) production is 1.1eV [9]. The energy gain raises the stress temperature to \(T_{max}\) from a reference temperature \(T_{ref}\) (298°K). Some of the energy released is consumed by recovery of the broken =Si- bond. Therefore, the temperature \(T(t)\) at any stress instant \(t\) can be modeled by sinusoidal wave [10], as given by:

\[ T(t) = \left[ (1/2)(T_{max} + T_{ref}) \right] + \left[ (1/2)(T_{max} - T_{ref}) \sin(2πft) \right], \]  (9)

where \(f\) is the thermal frequency. The temperature increment during the stress phase effects rates of sub-processes including D\(_{IT}\), D\(_{H2}\), k\(_{IT}\), k\(_{r}\), and k\(_{o}\); as described below.

#### Temperature dependence of diffusion rates

The diffusion sub-processes in oxide layer follows Fick’s law, e.g. D\(_{H}\) decreases linearly with decreasing H density from Si-SiO₂ interface. Alam used a simple approximation in the law, and suggested a triangular profile for D\(_{H}\) as shown in Fig. 2(b) [3]. Temperature impact on diffusion rates D\(_{IT}\) and D\(_{H2}\) is based on Arrhenius relation [13], which can be written as:

\[ D_H = D_{H,max} \exp \left( -\frac{E_a}{kT} \right), \]  (10)

where D\(_{H,max}\) is the diffusion rate at T\(_{ref}\), E\(_a\) is the activation energy, k is Bolzmann’s constant, and T is temperature. The equation describes H diffusion, but the same applies to H₂ diffusion. The diffusion variation with temperature change from T\(_{ref}\) to T\(_{(t)}\) is given by diffusion rates ratio [10]:

\[ \frac{D_H[T(t)]}{D_{ref}} = \exp \left[ \frac{E_a}{k} \left( \frac{1}{T_{ref}} - \frac{1}{T(t)} \right) \right], \]  (11)

The equation shows that the temperature increment increases D\(_{H}\), and hence accelerates N\(_{IT}\) generation. In order to account
for the additional $N_{IT}$ generated due to $D_H$ increment, an equivalent effective time ($t_{eq1}$) is calculated. $t_{eq1}$ is the time that the Si-SiO$_2$ interface would have taken to reach the $N_{IT}$ count in absence of $D_H$ variation [10]. The $t_{eq1}$ can be calculated as:

$$t_{eq1} = \frac{1}{D_{H_{ref}}} \int_0^t D_H[T(t)]\, dt,$$

$$= \frac{1}{D_{H_{ref}}} \int_0^t \exp \left[ \frac{-E_o}{k} \left( \frac{1}{T_{eq1}} - \frac{1}{T(t)} \right) \right] \, dt. \quad (12)$$

The remarkable feature of the above result is that temperature dependence of $D_{H}$ and $D_{H_{ref}}$ have been shifted to a time interval as shown in Fig. 3. For example the $D_{H}$ variation at $340^\circ K$ has equivalent time $t_{eq1}=30$ sec for $200$ sec stress time. In order to accommodate the diffusion variation in time domain, the stress will be applied for $230$ sec.

**Temperature dependence of conversion rate**

The PMOS negative gate stress breaks $Si-H$ bonds resulting in $≡Si-H$ bonds and H atoms. The H to $H_2$ conversion in SiO$_2$ is a complex mechanism, but we assume that the conversion takes place when an H atom approaches a $≡Si-H$ bond within a distance of $r_H<1.0nm$ [12]. Then we have:

$$≡Si - H + H ≡Si - H_2,$$  \hspace{1cm} (13)

where $k_H$ is the rate constant of H to $H_2$ conversion. The temperature impact on conversion can be understood by inspecting the rate constant $k_H$ [12], as given by:

$$k_H[T(t)] = 4 \pi D_H[T(t)] \cdot r_H \cdot \xi_1(x). \quad (14)$$

For atomic Hydrogen diffusion the parameter $\xi_1(x)$ is equal to $\sim 10^{-4}$. The equivalent time for acceleration in $k_H$ is calculated in same fashion as for $D_H$. The equivalent time $t_{eq2}$ is:

$$t_{eq2} = \frac{1}{D_{H_{ref}}} \int_0^t D_H[T(t)] \, dt,$$  \hspace{1cm} (15)

where $k_{H_{ref}}$ is the H to $H_2$ conversion rate at $T_{ref}$. Stressing transistor for additional $t_{eq2}$ will generate $N_{IT}$, equivalent to the count generated by $k_H$ variation.

**Temperature dependence of reaction rates ($k_f$, $k_r$)**

The RD model predicts that $N_{IT}$ generation during stress phase depend on $≡Si-H$ breaking rate ($k_f$), and $≡Si-$ recovery rate ($k_r$). The $k_f$ and $k_r$ dependence on temperature is [3]:

$$k_f[T(t)] \propto E_{ox} \cdot \exp(E_{ox}/E_o) \cdot \exp(E_a(k_f)/E_o) / kT(t),$$

$$k_r[T(t)] \propto \exp(E_o(k_r)/E_o) / kT(t), \quad (16)$$

where $E_{ox}$ is oxide field, $E_o$ is field acceleration constant, and $E_a(k_f)$, $E_a(k_r)$ are $k_f$ and $k_r$ activation energies respectively. The equation shows temperature increment increases $k_r$, that in turn increases $N_{IT}$ count. The equivalent time ($t_{eq3}$) for additional $N_{IT}$, due to $k_r$ acceleration is given by:

$$t_{eq3} = \frac{1}{k_{f_{ref}}} \int_0^t k_f[T(t)] \, dt,$$  \hspace{1cm} (17)

where $k_{f_{ref}}$ is reaction rate at $T_{ref}$. At intermediate and longer stress time, both $k_f$ and $k_r$ take place in parallel. Under these condition ratio between $k_r$ and $k_f$ is used, as given by [3]:

$$\frac{k_f}{k_r} \propto \exp(E_{ox}/E_o) \exp(-E_a(k_f) + E_a(k_r))/kT. \quad (18)$$

Simulation results supported by industrial data reveal that quick recovery of $≡Si-$ bonds during recovery phase is due to the fact that $E_a(k_f) \approx E_a(k_r)$ [3]. By considering $E_a(k_f) \approx E_a(k_r)$ Eq. 18 can be written as:

$$\frac{k_f}{k_r} \propto \exp(E_{ox}/E_o). \quad (19)$$

The equation shows that when $k_f$ and $k_r$ take place in parallel, the reaction rates become temperature independent.

**In conclusion**, Eq. [11,14,16,19] present the temperature impact on different sub-processes that contribute to NBTI degradation at different stages of the stress phase. The Eq. [12,15,17] transform temperature impact into corresponding equivalent times $t'$'s. Under such conditions $N_{IT}$ generated during the four stages [see section II], are given by:

$$N_{IT}(T(t)) = (k_f \cdot N_{IT}(t_{eq3})), \quad (20a)$$

$$N_{IT}(T(t)) = (N_{IT}(t_{eq3}) \cdot \exp(E_{ox}/E_o)^{2/3} \times (k_f \cdot t_{eq3})^{1/3} \times (t_{eq3})^{1/3}) \quad (20b)$$

$$N_{IT}(T(t)) = (N_{IT}(t_{eq3}) \cdot \exp(E_{ox}/E_o)^{1/2} \times (D_{H_{ref}} \cdot t_{eq3})^{1/4} \times (t_{eq3})^{1/4}) \quad (20c)$$

$$N_{IT}(T(t)) = (k_f/k_{H_{ref}})^{1/2} \cdot (t_{eq3})^{1/2} \times (D_{H_{ref}} \cdot t_{eq3})^{1/6} \times (t_{eq3})^{1/6} \quad (20d)$$

**B. Temperature Impact during Recovery Phase**

The exact recovery phenomena is not completely understood. However, two different views about this: (a) most of the H species are free inside the SiO$_2$ layer; during recovery phase the species diffuse toward Si-SiO$_2$ interface to recover the $≡Si-$ bond [14], (b) most of the H-species are locked by oxygen vacancy or atoms, and some are absorbed by the poly-silicon layer; during recovery phase the species unlock themselves and recover the $≡Si-$ bond [14].

In order to analyze temperature impact we consider both cases. Firstly, we assume that there are free H species available in SiO$_2$ layer. Recovery of $≡Si-$ bond take place when H species diffuse toward the Si-SiO$_2$ interface. Since diffusion of H species is involved, $≡Si-$ bond recovery is also function of temperature by following Eq. 10. Secondly, at room temperature the H species are locked, so their probability of release and diffusion is much lower, but at high temperature, these species may overcome a thermodynamic barrier, and diffuse towards the Si-SiO$_2$ interface to recover the $≡Si-$ bonds. However the exact mechanism is still not clear.
IV. SIMULATION RESULTS

We have modeled NBTI impact on PMOS transistor using temperature dependent external voltage source \( V_{\text{NBTI}} \) in HSPICE net list. Behavior of the source (defined by Eq. 20a-20d) is modeled using a Verilog-A module \( V_{\text{NBTI}} \) as shown in Fig. 4. Inputs to the module circuit are: temperature \( T(t) \), biasing voltage \( V_{dd} \), and transistor physical parameter \( T_{\text{OX}} \). The voltage across the module \( V_m(\pm) \) represents the PMOS threshold voltage increase, that causes hole mobility degradation and delay increment.

Simulations of NBTI degradation were carried out on 90nm CMOS technology with 1.2V biasing voltage and transistor temperatures in range \((25^\circ\text{C}-125^\circ\text{C})\). Fig. 5 validates the threshold voltage increment due to NBTI degradation. The figure shows that threshold voltage increment is temperature sensitive. The voltage increment after 10\(^3\) sec stress at 25\(^\circ\text{C}\) is 22.56 mV, and when the temperature increases to 125\(^\circ\text{C}\) during stress phase, the shift reaches up to 36.98 mV, causing 34\% additional shift. The results are consistent with [13] for short stress time under temperature variation, however at longer stress time our analysis predict less degradation due to lower time exponent for \( \text{H}_2 \) diffusion (see Eq.6).

![Fig. 4. The Verilog-A source representing NBTI degradation under temperature variation.](image)

The carriers mobility degradation due to NBTI is given in Table I. At lower temperature \( T_{\text{ref}} \), impact of interface traps is less dominant. Therefore, mobility variation with time is about 0.97\% for entire stress duration. However at higher temperature (125\(^\circ\text{C}\)) impacts of interface traps dominates and mobility degradation increases up to 11\%.

<table>
<thead>
<tr>
<th>Time (Sec)</th>
<th>Temp (25(^\circ\text{C}))</th>
<th>Temp (75(^\circ\text{C}))</th>
<th>Temp (125(^\circ\text{C}))</th>
</tr>
</thead>
<tbody>
<tr>
<td>10</td>
<td>0.16%</td>
<td>4.79%</td>
<td>7.20%</td>
</tr>
<tr>
<td>50</td>
<td>0.75%</td>
<td>6.30%</td>
<td>9.30%</td>
</tr>
<tr>
<td>200</td>
<td>0.86%</td>
<td>6.99%</td>
<td>10.23%</td>
</tr>
</tbody>
</table>

The decrease in mobility results in transistor delay degradation. In order to investigate temperature stimulated delay degradation due to NBTI for PMOS, we assumed a delay \( t_{\text{pdo}} = 14\text{ps} \) at \( T_{\text{ref}} \) as a reference. Fig. 8 shows delay degradation for different temperature at the end of 10\(^3\) sec stress. For \( T_{\text{ref}} \) the degradation in delay due to NBTI is about 0.15\%. The delay increases with rise in temperature. The figure shows that for same stress duration the delay increases by approximately 2.96\% at temperature \( T(t)=125^\circ\text{C} \).

![Fig. 6. Transistor delay degradation at different operation temperature.](image)

REFERENCES