Optimize your power and performance yields and regain those sleepless nights

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The challenges of managing energy efficiency and performance in SoC designs often result in sleepless nights searching for a solution. Today processors have to deliver more computational power, while maintaining flexibility and delivering the lowest power envelope simultaneously. These requirements are fundamentally contradictory in nature. This paradox keeps designers up at night trying to develop the perfect tradeoff between energy efficiency, flexibility and performance. This session will discuss some of the latest and most advanced techniques in power and performance management. Topics will include clocking, controlling idle and active power, optimizing data pipelines, hardware accelerators, advancements in microprocessor architecture and utilizing optimized libraries, mfg process, tools and design flow to ensure optimal power and performance ratios.

The challenges of low-power microprocessor design are unique in the sense that a significant power savings is desired with little or no performance and area impact. ARM has developed a series of optimized processor architectures and optimized libraries to provide the highest level of flexibility in meeting your area, performance and power requirements. In addition, they have worked with leading EDA companies, Foundries and Silicon Manufacturers to develop a complete design solution. This session will reference the ARM Cortex™ processor family and optimized ARM libraries to demonstrate the best-in-class strategies for designing optimal low power, high performance consumer devices.