Spintronic Memristor Devices and Application

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Abstract—Spintronic memristor devices based upon spin torque induced magnetization motion are presented and potential application examples are given. The structure and material of these proposed spin torque memristors are based upon existing (and/or commercialized) magnetic devices and can be easily integrated on top of a CMOS. This provides better controllability and flexibility to realize the promises of nanoscale memristors. Utilizing its unique device behavior, the paper explores spintronic memristor potential applications in multibit data storage and logic, novel sensing scheme, power management and information security.

Keywords—spintronic; memristor; spin torque; storage; sensing; power management; security.

I. INTRODUCTION

Memristor concept [1] recently received significant attention due to the demonstration of a practical nano-scale memristor device based upon ionic transport in resistive memory stack [2]. Originally proposed as the fourth circuit element for the completeness of circuit theory, memristance \( M \) denotes the relationship between magnetic flux \( \phi \) and electric charge \( q \):

\[
d\phi = Mdq. \tag{1}
\]

Memristor has very broad applications that include non-volatile memory, signal processing, control and learning system etc.

Nano-scale spintronic memristor has been proposed based upon spin torque induced magnetization motion [3] and spin transport at semiconductor/ferromagnet junction [4]. Realizing memristive effects in spintronic device not only provides understanding of a wide range of current-voltage behaviors observed in nanoscale spintronic system, but also sheds light on how we should look at existing/proposed magnetic devices and herald new applications. In this paper, based upon unique device characters of the proposed spintronic memristors, we explore their potential applications in multibit data storage and logic, novel sensing scheme, power management and information security.

II. SPINTRONIC MEMRISTOR THROUGH SPIN TORQUE INDUCED MAGNETIZATION MOTION

Memristor has unique electric behavior different from other circuit elements as resistance \( R \), capacitance \( C \) and inductance \( L \). Memristance can be calculated by:

\[
M(q) = \frac{d\phi}{dq} = \frac{V}{I}. \tag{2}
\]

although unit of memristance is the same as that of resistance – ohm \( (\Omega) \), the key difference between a memristor and a resistor is that memristance is a function of charge, which depends on the hysteretic behavior of current/voltage profile (or integral of current/voltage profile). The intrinsic constitution relation for memristor is charge versus flux. Memristor has unique ability to accumulate current/voltage information through constant current and/or voltage driving strength. As a comparison, in order to keep accumulating charge, the capacitor must be driven with a varying voltage. This is because the intrinsic constitution relation of capacitor is charge versus voltage.

For the proposed spin torque memristors [3], the resistance dependence upon integration of current/voltage is achieved through a combination of magnetoresistance and spin torque induced magnetization motion. The resistance of the proposed spintronic device is determined by its magnetization state through magnetoresistance principle. The magnetization state of the device is changed by current electron spin through spin torque induced magnetization motion. The final device magnetization state is determined by the accumulative effect of electron spin excitations. Thus device resistance depends upon the integral effects of current/voltage profile.

The physics process and scaling behavior of the proposed spin torque memristor are well understood. The required material for the device is similar to commercial recording heads material. This means the proposed device is controllable and tunable. Also the device can be easily integrated on top of CMOS. The integration of the spin torque memristor on CMOS is the same as integration of magnetic random access memory cell on CMOS. This has been achieved and commercialized in magnetic random access memory.

III. SPINTRONIC MEMRISTORSING APPLICATIONS

The unique spintronic memristor device behavior will be illustrated through potential application examples in multibit data storage and logic, novel sensing scheme, power management and information security.

A. Multibit Data Storage and Logic

Magnetic tunneling junction (MTJ) has been used in commercial recording heads to sense magnetic flux. It is the core device cell for spin torque magnetic random access memory [5] and has also been proposed for logic devices [6]. MTJ in these applications are generally viewed as a two
resistance states device. The resistance states are nonvolatile and the switching is achieved when reversal current/voltage magnitude passes a critical threshold. Based upon this view, MTJ is characterized as a nonlinear resistance through R-I or R-V curve.

However, as shown in [3], spin torque excited MTJ is a memristor. When the observation time reaches a scale that explicitly involves interactions between magnetization dynamics and electronics transport, the I-V curve (or widely used R-I curve) is not intrinsic to MTJ. MTJ resistance switching is determined by current/voltage profile. Here we will illustrate this point further through multi-bit MTJ and show this memristive behavior can be used for practical design.

MTJ multilevel cell spin torque switching has been demonstrated experimentally in [7]. Two multi-bit MTJ cell examples are presented. In the first example, two horizontal domains are introduced in MTJ free layer to generate four bits 00/01/10/11. In the second example, two MTJ are stacked vertically to generate four bits. Figure 1 shows schematically the switching behavior of these multi-bit MTJ cells through R-I curve. One bit of the two bits cell is hard and requires higher current to switch and the other bit is soft and requires less current to switch. Thus by varying switching current magnitude, individual bit can be switched. In the following we denote the first bit as hard bit and the second bit as soft bit.

Based upon R-I curve switching behavior, multi-bit MTJ cell has reversible branches and irreversible branches. For example, reversible transitions between 11 and 10, 01 and 00 can be achieved, however 00 state cannot be directly switched to 10 state using a single current pulse because switching the first bit requires higher current than switching the second bit.

Figure 2 shows examples of MTJ switching current magnitude versus pulse width. At nanosecond region, MTJ switching current magnitude is approximately proportional to the inverse of the pulse width. MTJ switching behavior is determined by integration of current pulse instead of current magnitude.

Figure 2. Switching current versus inverse pulse width for two multi-bit MTJ subcells

Two curves on figure 2 correspond to two MTJ sub-cells with same material. The two cells have different shape induced anisotropy and effective volume. The dot line sub-cell has more squared shape and bigger surface area while the square curve has more elongated shape and less surface area. The elongated sub-cell requires less current to switch at smaller current magnitude, however the switching speed of the elongated sub-cell is slower than that of the squared cell when current magnitude increases. As a result, two switching curves cross at current magnitude around 900uA and pulse width around 4nsec. If we denote the elongated sub-cell as soft bit, the two sub-cells of MTJ can be switched freely by using current with different pulse width. The longer current pulse width switches the soft sub-cell, corresponding to switching between 00 and 01 states. The shorter current pulse width switches the hard sub-cell, corresponding to switching between 00 and 10 states.

It is well known that memristor has rich dynamic behavior when excited with a dynamic current/voltage profile. The example here shows a practical application in multi-bit MTJ cell switching. By controlling switching current pulse width, the sub-cells of MTJ are designed to switch freely between different bits combinations.

B. Novel Sensing Scheme

For multi-bit MTJ cells, if the domain wall can be controlled to move and stop continuously across the free layer and/or many stable MTJ layers can be stacked vertically, the memory device can theoretically store continuous information through continuous resistance change. Memristors based upon spin torque induced continuous domain wall motion in ferromagnetic thin film was proposed in [3]. Application of the device for temperature sensor was pursued in [9].

The device structure for temperature sensor is in Fig. 3a. It consists of a long spin-valve strip which includes two
ferromagnetic layers: reference layer and free layer. The magnetization direction of reference layer is fixed by coupling to a pinned magnetic reference layer. The free layer is divided by a domain-wall into two segments that have opposite magnetization directions to each other. The device time domain resistance depends upon domain wall position as:

\[ R(t) = R_{H} - (R_{H} - R_{L})X(t)/D, \]

where \( R_{H} \) and \( R_{L} \) are the high and low resistance of the spin valve, \( D \) is the spin valve length and \( X \) is the domain wall position.

![Figure 3. Spintronic memristor through spin torque induced domain wall motion in spin valve structure (a) and magnetic tunneling junction structure (b)](image)

Domain wall velocity at finite temperature depends upon both spin torque excitation strength and thermal fluctuation magnitude. Fig. 4 shows the normalized domain wall velocity as a function of the normalized current density for different normalized thermal fluctuation magnitudes. Domain wall velocity increases as temperature increases. Temperature sensitive and insensitive regions can be observed. Curves with kneeling shapes are around critical current density, where the domain wall velocity is sensitive to thermal fluctuation magnitude. For temperature sensing, a biasing voltage pulse with constant magnitude is applied to the device. Resistance difference before and after voltage pulse is measured. This resistance difference is calibrated to sense temperature. Higher temperature results a bigger resistance dropping as shown in Figure 5.

The temperature sensing memristor is operated at a region where its electric behavior is sensitive to temperature change. This is achieved through a combination of temperature dependent domain wall mobility and the positive feedback between resistance and driving strength in memristor. The positive feedback between resistance and driving strength is a unique property of the memristor. Memristor’s resistance depends upon the integration of current/voltage excitation. For a constant voltage pulse driving, higher temperature results an increased domain wall moving distance. The increased domain wall moving distance results a smaller resistance. The smaller resistance results a higher driving current density, thus providing positive feedback to further increase domain wall distance. This positive feedback accelerates domain wall speed and reduces device resistance further for a constant voltage pulse driving. Solid curves on the Fig. 5 are the resistance changes for the proposed spintronic memristor at different temperatures. Dash lines are the resistance dropping for a non-memristive device without positive feedback between resistance and the integration of driving strength. The dash lines are equivalent to simulations with fixed driving current strength. It can be seen that positive feed back between resistance and driving strength in memristor significantly increases the temperature sensing margin.

![Figure 4. Normalized domain wall velocity as a function of normalized current density for different normalized temperature. Inserted figure shows the detailed velocity versus current density at temperature sensitive region around critical current density.](image)

For the example case shown in Fig. 5 (detailed parameters are in [9]), the temperature sensing range is from 300K to 400K, which covers the normal operation range of semiconductor chip. The required power supply voltage is 0.3 volt with a typical power consumption of 150uW. The linearity is 0.5Ohm/degree and the surface area is 300nm x 20nm. Compared to the available on-chip temperature sensors, the device requires much lower power supply voltage (which can be even used in the sub-threshold voltage region) and power consumption (compared to some on-chip oscillation-ring-based temperature sensor that consumes huge dynamic power), nano-scale feature size, low cost and the mature integration technology with CMOS process. The device is targeting the highly integrated on-chip thermal detection applications, e.g., cell size < 1um2.

The operating range and device properties can be further tuned according to practical needs and material capabilities, e.g., the thermal effects in the device scale as temperature over domain wall thickness. Varying domain wall thickness through tuning magnetic material properties could change device temperature operating range. Linearity or resolution of the device can be improved by utilizing magnetic stack with high GMR (giant magnetoresistance) or even TMR (tunneling magnetoresistance) stack. The Magnetic tunneling junction structure with spin torque induced free layer domain wall motion is shown in figure 3(b). Magnetic tunneling junction (MTJ) usually includes two ferromagnetic layers and one oxide barrier layer (e.g., MgO). The magnetoresistance ratio (defined as resistance difference divided by low resistance) of the commercialized MTJ can be above 100%. For MTJ, the driving current is perpendicular to the stack and the two resistors due to
different magnetization orientations are connected in parallel. The MTJ free layer domain wall moves due to spin torque of free electrons polarized by the fixed magnetization in the reference layer. Resistance change due to MTJ free layer domain structure change has been shown experimentally in [7].

Spintronic memristor has remarkable characters to sense nano-scale temperature. This is because of following unique properties of ferromagnetic system and memristor device. Ferromagnetic material is special for its stable coherent macroscopic ordered states, such as multi-stable magnetization states, domain wall structure etc. Understanding and manipulating these structures have led to rapid growth of magnetic information storage capacity. As magnetic device scales down, we are now engineering magnetic coherent structures at nano-scale that explicitly interact with thermal fluctuations. The interactions between macroscopic coherent magnetic structures and thermal fluctuations in ferromagnetic material provide the opportunity for nano-scale temperature sensing. Memristor device is special for this application because it is an integration system. In the proposed memristor temperature sensing, thermal fluctuations are integrated through thermally assisted domain wall motion in magnetic thin film. The positive feedback between memristor resistance and driving strength is the key for this application.

Figure 5. spintronic memristor resistance as a function of time at different temperatures (300K, 350K, 400K) for a constant magnitude voltage pulse driving.

The unique ferromagnetic spintronic memristor device characters can be used for other novel sensing scheme. Besides temperature sensing, spintronic memristor can be designed to sense current fluctuations, electromagnetic field fluctuations and even material defects. The integration capabilities and positive feedback mechanism in spintronic memristor make it particularly suitable for sensing random and fluctuating events. Nano-scale feature size, low cost and the mature integration technology with CMOS are the main advantages for their practical applications.

C. Power Management

The ability to accumulate current/voltage through constant current and/or voltage driving strength makes memristor suitable for power monitor. Figure 6 shows connecting a memristor to a circuit either in series or in parallel. For connecting memristor in series with circuit (Fig. 6a), the whole system is powered by a constant voltage V. The energy consumed by the whole system, including both memristor and circuit, is calculated as: $E = \int Vdt = V \int Idt$. Integration of current $\int Idt$ can be read out by memristor resistance. Since V is known, the energy consumed by the whole system can be read out. To minimize the impact of memristor, the memristance of memristor is required to be much smaller than the resistance of circuit.

For connecting memristor in parallel with circuit (Fig. 6b), the whole system is powered by a constant current I. The energy consumed by the whole system, including both memristor and circuit, is calculated as: $E = \int Vdt = I \int Vdt$. Integration of voltage $\int Vdt$ can be read out by memristor resistance. Since I is known, the energy consumed by the whole system can be read out. To minimize the impact of memristor, the memristance of memristor is required to be much bigger than the resistance of circuit.

To read out the value of memristance, same as any resistance read method, a current or voltage can be applied to memristor. The generated corresponding current or voltage is compared to a reference for resistance value detection, as shown in Fig. 6c. Such a read operation may disturb the state of memristor. To recover the state, an opposite current or voltage with same time duration can be applied.

Figure 6. memristor based power monitor (a) (b) and memristance sensing (c).

Besides passive power monitor, spintronic memristor can also be used to actively control circuit power. The negative feedback between memristor resistance and power is the key for this application. In the previous spintronic memristor
temperature sensing scheme, the domain wall moves in a direction to reduce device resistance. For a constant voltage pulse driving thermally assisted spin torque domain motion, a positive feedback forms between increasing temperature and decreasing resistance. For active circuit power control, a negative feedback is required between power increasing and memristor resistance increasing.

Let’s consider the example of Fig 6 (a), where a memristor connects to a circuit in series. Instead of much smaller negligible memristor resistance as in the case of power monitor, for active power control, memristor resistance is comparable to that of the circuit. For a constant voltage driving, increasing memristor resistance reduces the current passing through the circuit, resulting less circuit power. For active power control, the domain wall of memristor moves in a direction to increase memristance. When the circuit power increases, memristor domain wall is pushed toward a direction to increase the memristor resistance. This reduces the current and power through circuit. A negative feedback forms between memristor resistance and circuit power. Notice here the resistance is not a function of current but a function of the power (integration of the current).

D. Information Security

I will present spintronic memristor device designs that serve the following purpose: when a user reads the data information stored in the device, the administrator who wrote the data knows immediately if he/she checks the device. The advantage of spintronic memristor in information security is due to its resistance dependence upon historic current/voltage profile behavior. In order to access the data stored in a spintronic memristor, the user must excite the device electrically. This excitation activity can be memorized in a memristor and later be revealed for security check.

A successful designed scheme must be able to fight against following action. After reading the stored data information, the user tries to restore the device state to the same state as before reading, so that administrator could not find whether the data has been accessed. One key point here is whether the user is given the limited or the same authority on device writing and reading compared to that of the administrator. For the case of user with limited reading and/or writing authority, data information security task can be more easily achieved. For limited writing authority case, user may not be able to restore the device to the state set by the administrator before. For reading limited case, the user may not know the state of the device set by the administrator.

I will present a scheme for the case that user and administrator has the same authority on writing and reading. For the writing process, administrator sets high resistance state (0) fully saturated and low resistance state (1) partially saturated. (For a finite size free layer, when the domain wall reaches the free layer boundary, the device is saturated. Otherwise it is partially saturated). The reading process is special here. It is achieved by two constant voltage pulses, one pulse tries to push domain wall toward high resistance end and the other pulse tries to push domain wall toward low resistance end. The two pulses excite device several times (in the order of 10) times during reading. The device reports two values for reading: 1) final state of the device close to high or low resistance state (High or Low) and 2) whether the device resistance has been significantly changed during reading (Yes or No).

A simplified analytical model is presented here to illustrate device working principle. The device is a magnetic tunneling junction as shown in Fig 3(b). In the following, all the formulas are normalized. The domain wall velocity as a function of current strength follows a curve similar to Fig. 4. In temperature insensitive region, it is approximated as:

\[ v = \begin{cases} 
0, & I \leq 1 \\
\frac{I}{\sqrt{7I-1}}, & I > 1 
\end{cases} \]  

(3)

The resistance of device is determined by domain wall position \( x \) (\( 0 \leq x \leq 1 \), normalized by device length):

\[ R = \frac{R_{\text{min}}(1+TMR)}{1+TMRx} \]  

(4)

It is the resistance of two parallel connected resistors with resistance \( R_{\text{min}}(1+TMR)/(1-x) \) and \( R_{\text{min}}/x \). When driven by a constant voltage, the current magnitude is:

\[ I = 1.5\beta \frac{1+TMR}{1+TMR} \]  

(5)

where \( \beta \) determines the voltage pulse magnitude. For TMR=1, the domain wall velocity combining (3) and (5) is:

\[ \frac{dx}{dt} = v = \begin{cases} 
0, & x \leq 2-1.5\beta \\
\frac{1.5\beta}{2-1.5\beta} & x > 2-1.5\beta 
\end{cases} \]  

(6)

Integration of (6) gives final domain wall position as a function of the initial domain wall position and pulse width \( T \):

\[ x_f = f(x_i, \beta, T) = 2 \left[ T + \frac{4}{1.5\beta} \left( \frac{1.5\beta}{2} - 1 \right) \frac{1.5\beta}{2} - 1 \right] - (1.5\beta - 1) \]  

(7)

when \( \beta > 2/1.5/(1+x_i) \) and \( x_f = x_i \) when \( 0 < \beta < 2/1.5/(1+x_i) \). The analytical formula \( f(x_i, \beta, T) \) for negative driving current \( \beta < 0 \) can also be obtained similarly.

For this device example, when domain wall position \( x \) is bigger than 0.3, the device is readout as low resistance state and we denote the domain wall position as close to low resistance end. When domain wall position \( x \) is smaller than 0.3, the device is readout as high resistance state and we denote the domain wall position as close to high resistance end. For writing procedure, domain wall position is set to zero for fully saturated high resistance state and domain wall position is set to be bigger than 0.3 for partially saturated low resistance state.
For reading procedure, the first reading pulse has fixed pulse width $T=0.1$ and fixed magnitude $\beta = -1$. The second reading pulse has a fixed smaller pulse width $T=0.4$ and varying pulse magnitude. The second pulse magnitude can be controlled by user and administrator. When two voltage pulses are exerted on the device several times (order of 10), for partially saturated low resistance state ($x>0.3$), the domain wall position settles to a fixed point. This fixed point changes as the second pulse driving strength. Figure 7 shows the fixed point as a function of the second pulse driving strength. Notice also for the current magnitude range in Figure 7, when the device is in saturated high resistance state, the reading pulses can not move the domain wall to low resistance state.

![Figure 7](image)

The working principle of data information security is as follows: the administrator fully saturate high resistance state and partially saturate low resistance state. When the administrator reads the data, he/she uses pulses with a particular second pulse driving strength. After first reading the data, the domain wall settles to a particular position. Now if the device is read by a pulse with the same second pulse driving strength, the domain wall position is fixed and the device will reports No to resistance change reading. Notice the administrator can also set the bit by one writing without reading if he/she uses the writing current to move the domain wall to the position corresponding to the fixed position of particular reading second pulse strength.

Now if the device is read by a pulse with a different second pulse driving strength, the domain wall position is changed. For the user who does not know the second pulse strength used by the administrator, reading the device with an arbitrary different second pulse magnitude will move the domain wall to a different position. Later when administrator checks the device using the known second pulse strength, the domain wall moves back to its initial position and the device reports Yes regarding resistance change. By checking the Yes or No on resistance change reading, the administrator knows whether the device information has been accessed.

In order to fight administrator’s checking, user must find the domain wall position set by the administrator using a particular current strength. The user must be able to achieve this for the first time he/she reads the device. This is because during the first reading, if the second pulse driving strength is different from that of administrator, the domain wall position is changed and the information on domain wall position set by administrator is lost. Guessing a particular number in a continuum range would be almost impossible for the user.

Of course if the administrator uses the same second pulse width for all the cells, the user could try many different second pulse driving strengths on many different cells to figure it out. However administrator has no reason to use the same second pulse driving strength for all cells. Any random second pulse driving strength scheme will beat user’s attempt to hide his reading device activity.

For the device example shown here, in the case of user with limited writing and/or reading authority, the scheme is simplified significantly. For limited writing authority, if the user is only allowed to fully saturate the device, he/she can then not restore the partially saturated state set by administrator. For limited reading authority, if user only gets the information of High or Low resistance state without obtaining Yes or No information on resistance change, he/she do not know the domain wall position set by the administrator.

A particular design example is given here to illustrate spintronic memristor possible application in information security. There could be many different approaches and for the scheme proposed here, there are also many issues regarding writing/reading margin and system optimization. These will be deferred to further publications.

REFERENCES