

# EMC-aware Design on a Microcontroller for Automotive Applications

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## Abstract

*In modern digital ICs, the increasing demand for performance and throughput requires operating frequencies of hundreds of megahertz, and in several cases exceeding the gigahertz range. Following the technology scaling trends, this request will continue to rise, thus increasing the electromagnetic interference (EMI) generated by electronic systems. The enforcement of strict governmental regulations and international standards, mainly (but not only) in the automotive domain, are driving new efforts towards design solutions for electromagnetic compatibility (EMC). Hence, EMC/EMI is rapidly becoming a major concern for high-speed circuit and package designers. The on-chip power rail noise is one of the most detrimental sources of electromagnetic (EM) conducted emissions, since it propagates to the board through the power and ground I/O pads. In this work we investigate the impact of power rail noise on EMI, and we show that by limiting this noise source it is possible to drastically reduce the conducted emissions. Furthermore, we present a transistor-level lumped-element simulation model of the system power distribution network (PDN) that allows chip, package, and board designers to assess the power integrity and predict the conducted emissions at critical chip I/O pads. The experimental results obtained on an industrial microcontroller for automotive applications demonstrate the effectiveness of our approach.*

## 1. Introduction

The continuous shrinking of the device feature sizes introduced by aggressive technology scaling trends, and the increasing complexity of digital ICs, require higher operating frequencies with faster clock rates. Because of high-frequency square-waves rich in harmonics and distributed throughout the die, ICs are becoming prolific EMI generators. However, until recently, circuit, package, and board designers did not give much consideration to EM emissions and interference. Traditionally, the problem of reducing on-chip EMI has been more an art than a science, and different engineering solutions were considered, tested, and implemented by *trial-and-error*, without any structured approach. Such

an avenue was mainly followed by practitioners, as there is a lack of circuit designers in the VLSI community, who also have a solid technical background in EMC/EMI. In fact, when the on-chip EM emissions exceeded the level imposed by either the international legislation or by customers (mainly in the automotive domain), patches and workarounds could be found on the printed circuit board (PCB) by inserting off-chip decoupling capacitances in close proximity of the die noisy I/O pads. Obviously, this approach is no longer acceptable, since the international standards and regulations [1][2], the customer's requirements, and an increasingly aggressive competition in the automotive market dictate a deep theoretical understanding of the EMC/EMI problem. Moreover, a systematic method to deploy effective and reusable solutions for a wide range of applications, an accurate and practical modeling approach for the system PDN to estimate the system power integrity and EMC behavior before fabrication, and the development of an overall EMC-aware design methodology that addresses EMI reduction during the top-down design flow, are also necessary to avoid costly design re-spins. EMC has become another critical objective for first-silicon success. In fact, even if the traditional constraints such as area, timing, and power consumption are satisfied, but the chip does not meet the EMC requirements, then the circuit has to be re-designed with a dramatic increase in terms of NRE costs, and subsequent delays in the product chain, thus missing critical *time-to-market* windows.

The most effective method to reduce on-chip EM emissions considers the switching current waveform generated on the power grid. The simultaneous toggling of logic gates and macroblocks typical of synchronous circuits results in narrow current glitches on both power supply and ground rails localized in close proximity of the clock edges. These pulsed currents are conducted off-chip through the I/O pads, thus driving the unintentional emitting antennas composed of the PCB traces and cables. Adequate power rail noise suppression is a critical requirement for the successful design of today's microelectronic systems, and it necessitates among other things the availability of low-impedance on-chip decoupling capacitors (i.e., decaps) to provide electric charge locally to the switching circuitry. In this work, we present an automatic design methodology for decap

insertion and power rail noise minimization, which can be seamlessly integrated into the standard design flow. This approach has been exploited to successfully reduce on-chip EMI on an industrial microcontroller for the automotive market.

Another essential component of an EMC-aware design methodology is the availability of an EMI simulation flow, which allows designers to efficiently and accurately evaluate the power integrity and EMC behavior of the die before tape-out considering the other system components such as the package and board. In fact, by neglecting the PCB traces loading effects when evaluating the chip power integrity and EMC performance, not only we will obtain inaccurate results with respect to post-fabrication measurements, but we will also ignore and overlook potentially critical design weaknesses, thus losing the fidelity between the EMI reduction and optimization techniques used during design, and their actual effectiveness measured after fabrication. In this paper, models of the IC core, package, and PCB were generated using commercial tools, and were used to predict the voltage noise at the power supply I/O pads and then estimate the electromagnetic conducted emission level.

This paper is organized as follows: Section 2 overviews some relevant previous work on power rail noise suppression, while the methodology for decap characterization and insertion is introduced in Section 3. Section 4 describes our system PDN modeling technique and EMI simulation flow, while Section 5 presents the experimental results validating the effectiveness of the proposed approach. Finally, Section 6 summarizes a few conclusive remarks.

## 2. Previous Work

In high-performance microcontrollers and cores, clock rates are steadily increasing, forcing very fast rise/fall times, and clocking to be strongly synchronous all over the chip. This means that all clock edges occur at the same time, thus causing large current pulses on the PDN and increasing the chip EMI [3]. Since fast current variations have a large harmonic content, a detrimental factor for EMC is the power rail noise or *simultaneous switching noise* (SSN) caused by the dynamic power and ground rail current fluctuations. In [4] it was demonstrated that SSN is originated mainly from package parasitic inductance, and with the increasing circuit frequencies and decreasing supply voltages, it is becoming more and more important [7][8][9]. The impact of SSN on the EM emissions of digital circuits was discussed in [5], and in [6] an approach to analyze the on-chip power supply noise for high-performance microprocessors was presented. Because the dynamic SSN is a major source of EMI, to develop an effective EMC-

aware design methodology, it is necessary to insert decoupling capacitors in proximity of current-hungry blocks [10]. In [11] a systematic study to understand the effects of off-chip and on-chip decoupling on the radiated emissions was presented. It was demonstrated that off-chip decaps are effective at reducing the EM radiation in the low-frequency range, while they do not have any significant impact in the high-frequency region. In contrast, on-chip decoupling is a valuable technique to suppress the EM radiation in the high-frequency region, and by a careful combination of off- and on-chip decoupling it was possible to achieve a significant suppression of EM emissions over the whole frequency spectrum. A qualitative assessment on the relative impact of design techniques to reduce on-chip EMI was presented in [12], to help designers making effective decisions at an early stage in the design process.

## 3. Decap Characterization and Insertion for Low-EMI Design

The fundamental issue is how many decaps should be used and where they should be placed. This matter becomes particularly pressing in today's SoC designs, especially in the automotive domain, where critical requirements such as a fast time-to-market and challenging silicon area constraints must be met by the design teams. Therefore, not only it is important to understand the effective behavior of intentional on-chip decaps, but it also mandatory to efficiently place them. It was confirmed through measurements [4][13] that on-chip decaps are efficient only when placed within a short physical distance from the switching components (standard cells, macroblocks, and I/O drivers) and noise sources. Indeed, with stringent area limits it is not possible to over fill the die with extra decaps, since there may not be enough white space available on the floorplan. Decaps are allocated either by surrounding each macroblock or by targeting specific edges of the macro bounding box. Edge targeting is useful when the switching activity is known to be highly non-uniform and confined primarily within regions near specific circuit boundaries (for example the sense amplifiers or the I/O drivers of the memories). This approach becomes much more important for those area-limited applications, where in order to effectively reduce the noise propagating through the I/O power supply pads, it is necessary to maximize the damping effect of the decoupling capacitances.

In SoC design, decaps are realized with fillercap cells (i.e., fillercaps), which are implemented by MOS transistors with long and wide channels to obtain sufficiently large capacitance values. The transistor works as a capacitor connected between the power supply ( $V_{DD}$ )

**Table 1. Fillercap cell characterization**

<i>Typical case</i> ( $V_{DD}=1.8V$ , $T=25C$ )	FILLER16	FILLER32	FILLER64
Nominal Cap Value (fF)	94.77	237.24	522.16
Cut-off Cap Value (fF)	67.01	167.75	369.22
Cut-off Frequency (GHz)	10.47	2.14	0.51

and ground with the top plate corresponding to the MOS device gate and the bottom one is the inversion layer. The time response of such fillercaps is crucial because of the short switching times, where the circuit components require a large amount of charge in a very brief time interval (typically a few tens of picoseconds for more recent technologies). Therefore, in such a small period of time, fillercaps have to be considered as distributed elements, since their timing constant can be larger than the switching time. The analysis performed in [15] demonstrated that at high working frequencies, the effective capacitance value of the MOS gate decreases. This detrimental effect is much more relevant for large fillercaps, implemented with MOS transistors with a long channel. At high frequencies, only a fraction of the channel close to the source and drain electrodes follows that gate voltage variation, while most of the channel remains isolated. As a consequence, the effective capacitance decreases, and the effectiveness of the fillercap cell is reduced.

The microcontroller considered in this work is the STXX, which was taped out in  $0.18\mu\text{m}$  embedded Non-Volatile Memory (eNVM) CMOS technology, with the NVM devices shrunk to  $0.13\mu\text{m}$ . The area constraints were very tight, and it was critical to maximize the decoupling effect of each fillercap. Therefore, it was necessary to use only those cells that did not suffer from capacitance value degradation due to the frequency increase. A frequency characterization of the fillercaps available in the library was performed for best-, worst-, and typical-case, and the results obtained on the most relevant cells in typical-case ( $V_{DD}=1.8V$ ,  $T=25C$ ) are summarized in Table 1. The operating frequency of the microcontroller was 24MHz, which is at least one order of magnitude below the cut-off frequency (where the effective capacitance value is  $-3dB$  with respect to the nominal value) of the fillercaps in Table 1 (this is also confirmed for best- and worst-case, whose results are not reported). Hence, even the large decaps were not subject to any effective capacitance decrease, and they could be used to reduce the on-chip EM conducted emissions, when enough white space was available around the noise sources.

After decap placement, a full-chip transient power noise simulation and EMI analysis based on the spectral

content obtained with FFT [14] was carried out to validate the effectiveness of fillercap insertion.

## 4. System Power Distribution Network Modeling

Power integrity requires a smooth delivery of supply currents without fast current transients that would generate high EMI while propagating into the surrounding electronic system. Reliable EMI models become mandatory to evaluate the system EMC performance prior to fabrication. Not only IC designers demand EMI models before tape-out, but also PCB designers using these ICs ask for EMI models to evaluate the board power integrity.

The system-level power integrity and EMC behavior can be evaluated with a circuit lumped-element model suitable for transistor-level simulations shown in Figure 1, which includes the voltage regulator module (VRM), the PCB planes and traces, the package lead frames and bond wires, the chip power grid rail parasitics and its switching current. The off-chip capacitors are usually represented as an ideal capacitor with an effective series resistance (ESR) and effective series inductance (ESL) modeling the parasitics of the capacitor package, where larger capacitors have larger effective series inductances.

The voltage regulator seeks to reproduce a constant output voltage independent of the load current, and in Figure 1 it is represented by an ideal voltage source in series with a small resistance and inductance of its pins. Usually near the VRM there is a large bulk capacitor (typically electrolytic or tantalum). Power ground planes on the PCB carry the supply current to the package, contributing some resistance and inductance. Typically the board designer places several small ceramic capacitors near the package critical pins. The package and its pins introduce some parasitic resistance and inductance. It is important to notice that high-frequency packages often contain small capacitors inside the package for further decoupling. Finally, the chip connects to the package through solder bumps or bond wires, with additional resistance and inductance. The chip lumped-element equivalent model includes the contribution of the I/O pads, the power grid rail parasitic resistance, and the bypass (i.e., decoupling) capacitances. The dynamic and static current demands of the chip are modeled as a variable current source. The on-chip bypass capacitance consists of the symbiotic (or intrinsic) capacitance and possibly some explicit decap due to the fillercap insertion, as it was discussed in Section 3.

A critical component of the system PDN model is the chip switching activity. In our EMC-aware design flow we used the Apache's tool suite (RedHawk and Senti-

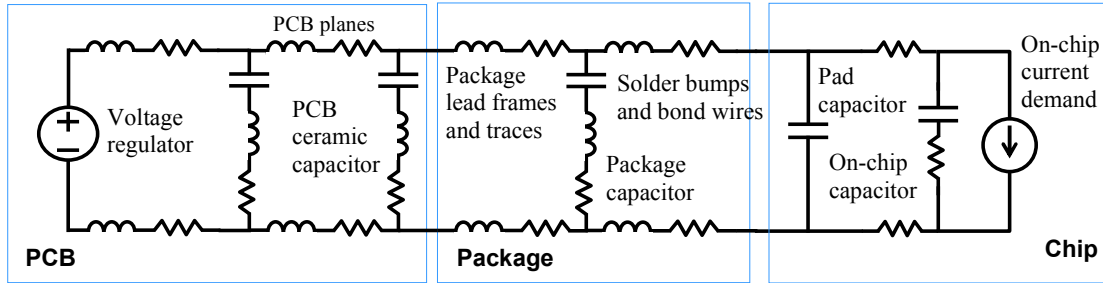


Figure 1. System power distribution network model

nel-CPM), which can generate a lumped SPICE-compatible chip power model (CPM) composed of the current waveform generator along with the die equivalent impedance network seen at a given pin or pin group. RedHawk/Sentinel-CPM can simulate the dynamic current behavior of the entire SoC. The current profile of each library cell is characterized with a circuit simulator taking into account the input transition time and output load capacitance of the cell library timing characterization grid. The determination of an accurate current signature for each component is one of the most difficult aspects of power rail noise estimation. In particular, for complex and large macros such as eNVM blocks, the current profile must be derived from a specific characterization. In our approach, this current signature is determined with Apache's Totem-MMX, either using the memory validation stimuli, or the VCD file obtained from the logic simulation. In order to derive the SoC's CPM, a vector-based set of stimuli such as the VCD file is preferred. However, a realistic simulation can also be achieved with some behavioral specification such as the full-chip/block/cell toggle rate and power consumption.

The package model was extracted considering the quasi-static assumption and using the Ansoft's Q3D tool. The physical length of the bond wires and the signal bandwidth of the application affect the frequency range validity region for using the quasi-static approach. In fact, the ratio between the maximum length of the package interconnection ( $L$ ) and the wavelength ( $\lambda$ ) of the application plays the major role for package modeling. An iterative algorithm divides the package 3-D structure into a mesh and calculates the electromagnetic field in each element to obtain the final result. The SPICE model of the package including resistance, self inductance, and self capacitance of each connection, as well as mutual inductances and coupling capacitances, is derived from the computed field quantities. When  $L < \lambda/10$ , the quasi-static approach is correct and each lead frame and bond wire can be described through RLC cells (lumped-element model), and the analyzed QFP package respects the above limitations.

In contrast, if  $L > \lambda/10$  then the quasi-static approach is no longer acceptable as propagation phenomena appear on the interconnections. In this case, the full wave approach without any frequency limitation is needed.

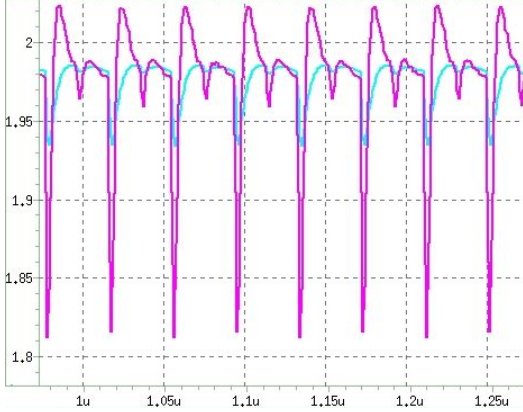
Finally, the PCB model was obtained with Sigrity's PowerSI and Broadband SPICE tools. Since the board of the automotive microcontroller considered in this work included an off-chip VRM, first we built a linear model of the VRM following the approach described in [16]. Subsequently, such linear model was included into the PCB description imported in PowerSI. In this way, the PCB lumped-element model obtained with Sigrity's tools included the filtering effect of the off-chip VRM.

The system PDN model illustrated in Figure 1 can be used to simulate the power integrity and EMC performance of the microcontroller considering the loading and parasitic effects of the complete system.

## 5. Experimental Results

Typical microcontrollers for automotive applications include analog and mixed signal blocks, eNVM memories, I/O circuitry, and a large digital core that usually takes electric energy from an independent power supply net. The need to keep the digital power grid separated from the other building blocks stems from the necessity to minimize the crosstalk between noisy circuits like the digital core and susceptible analog circuitry. In particular, the STXX is a microcontroller that contains a digital core with a separated power supply network of 1.8V, a large 128K-byte eeprom, two SRAMs, one ROM, and a few analog circuits, where the most important one for power consumption is the analog-to-digital converter.

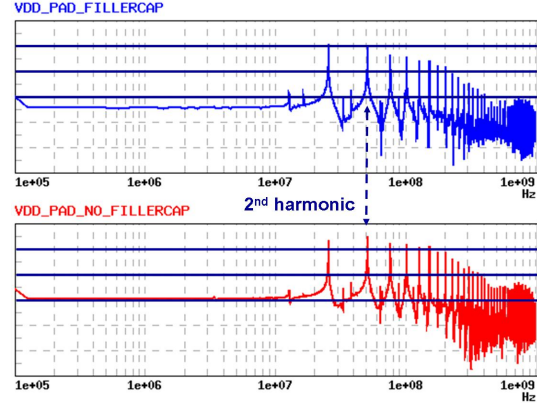
Because the memories and the analog macros are a significant portion of the STXX in terms of power consumption, to perform an accurate full-chip evaluation of the power rail noise, and consequently of the EM conducted emissions, their current profile must be obtained. This dynamic model should capture the current waveforms as well as parasitics for all the modes of the block (e.g., different modes of operation for a memory are the read/write/test modes). In our methodology, the current signatures of the hard macros can be generated by either



**Figure 2. Power rail noise waveforms at the power supply I/O pad**

using the VCD input or a probabilistic vector-less analysis. Since most of the macroblocks are too large, their characterization with a traditional circuit simulator is impractical. Hence, the dynamic current waveforms at each device that is connected to power and ground nets are obtained with a fast circuit simulator based on a set of input simulation vectors. The characterization engine extracts the effective intrinsic or intentional capacitance, equivalent resistance, and time-variant and voltage-dependent current models for each transistor-level device. While for large analog and mixed-signal (AMS) blocks (like the eeprom memory) it is necessary to obtain an accurate current signature, for smaller AMS circuitry, whose power consumption is negligible with respect to the power dissipated by the larger blocks, it may not be essential to derive such an accurate current profile, given that the corresponding characterization effort will be quite significant. As such, we considered these small macros simply as “*black boxes*”, and we obtained the equivalent impedance of their power grid that was connected to top-level power grid. In this way, the loading effects of these circuits were taken into account in the PDN of the overall SoC.

The fillercaps (a few of them are shown in Table 1) were inserted in the STXX floorplan for a total amount of 2.2nF, mostly in close proximity of the large memories, where the preliminary dynamic power analysis showed the power rail noise hotspots, without introducing neither area nor timing penalties. The noise reduction at the  $V_{DD}$  I/O pad of the digital core PDN was about 12mV (azure plot in Figure 2). Therefore, also achieved was a significant EM conducted emission attenuation, as illustrated in Figure 3, where the blue spectrum corresponds to the EMI analysis carried out after fillercap placement and optimization, and shows a significant and consistent decrease in harmonic magnitude across the overall frequency range (from the fundamental frequency at 24MHz up to 1 GHz). In particu-



**Figure 3. Power rail noise frequency spectra at the power supply I/O pad**

lar, at the second harmonic (48MHz singled out by the vertical dashed line) the harmonic amplitude reduction was 9.9dB $\mu$ V. The IC lumped-element model (i.e., CPM) was used for a fast assessment of the fillercap insertion. The critical requirement of this model was its accuracy with respect to the gate-level analysis, to drive the power rail noise minimization, allowing the designer to efficiently evaluate the amount of extrinsic on-chip decoupling capacitance necessary to achieve a target noise reduction. The waveforms reported in Figure 4 demonstrate an excellent accuracy between the transistor-level simulations with CPM, and the gate-level analysis performed with RedHawk. First, with CPM we determined the amount of fillercaps necessary to significantly reduce the voltage fluctuations at the power supply I/O pad of the digital core, and then we optimally distributed the 2.2nF decoupling capacitance in close proximity of the most critical noise sources.

Lastly, the impact of on-chip decoupling was also evaluated at the PCB pin where the conducted emission measurements are performed. The results are reported in Figure 5 and summarized in Table 2. It can be observed a consistent harmonic amplitude reduction within the frequency range up to 1GHz, thus demonstrating the effectiveness of our EMC-aware design and simulation methodology.

## 6. Conclusions

In this work we have presented a design methodology based on decoupling capacitance insertion and optimization to reduce on-chip EMI. In particular, our approach achieved a significant attenuation in EM conducted emissions, and we successfully exploited this methodology to tape out an industrial microcontroller for automotive applications with tight area constraints and critical EMC requirements. We integrated this methodology into the standard design flow, and demon-

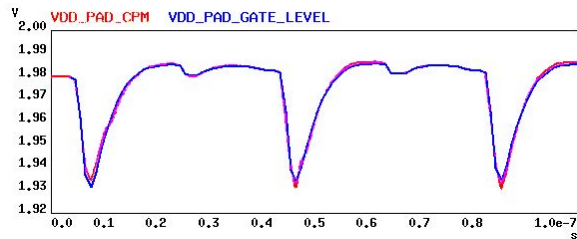


Figure 4. Gate-level analysis vs. CPM simulations

stated that it is possible to consider EMC during the design steps of complex industrial SoCs. Moreover, we also developed a system PDN model that was exploited in the design optimization phase, to efficiently estimate the amount of decoupling capacitance necessary to significantly decrease the noise at the power supply I/O pads, and at the PCB pin where the conducted emission measurements are performed. The experimental results on the STXX confirm the effectiveness of our methodology at reducing the chip electromagnetic emissions.

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Table 2. Harmonic amplitude reduction at PCB pin for conducted emission measurements

Harmonic	2	3	4	5	6	7	8
MHz	48	72	96	120	144	168	192
Amplitude Reduction (dB $\mu$ V)	9.0	11.0	13.8	14.1	14.7	14.2	14.3

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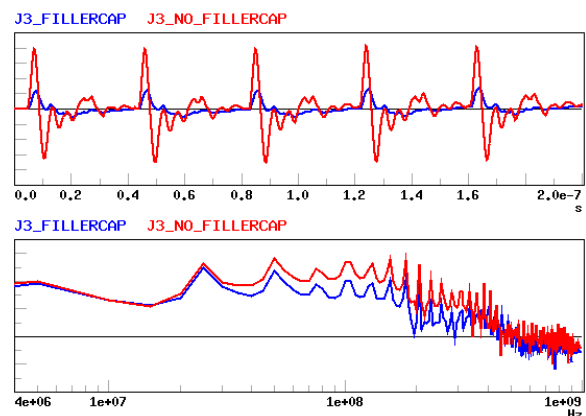


Figure 5. Noise waveforms and EMI spectra at PCB J3 pin for conducted emission measurements (w/o and w/- decaps)