

Verification of the RF Subsystem within Wireless LAN System Level Simulation

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Abstract

Today's mobile communication systems use sophisticated signal processing to achieve high transmission rates. Therefore a high complexity in the digital system part as well as very accurate signal processing in the analog RF subsystem is needed. So far analog and digital part are developed separately. The increased performance requirements demand now a common verification of the complete system including analog and digital parts. At the design of an IEEE 802.11a wireless LAN receiver it is demonstrated, how the RF receiver part is tested in the system level simulation. Different simulation tools are used. The simulation results show the impact of properties of the RF part on the system performance. Experiences from the tool evaluation are presented.

1. Introduction

The demand on mobile communication has grown over the last years. Starting with voice communication now mobile data transfer becomes more and more important. One of the fastest-growing application are the wireless local area networks (WLAN) which can extend or replace traditional wired computer networks. WLAN provides more flexibility, because network components can be placed somewhere in the WLAN range without cable installation. WLAN systems providing data rates up to 11 Mbit/s are widely used today. New standards (high-speed WLAN) will extend the transmission rate up to 54 Mbit/s.

High transmission rates within band limited radio channels affect the growing complexity of the devices and require the following:

- very high transmission frequencies must be used
 - sophisticated modulation and coding technologies are used to achieve a high spectral efficiency
 - high requirements for the RF front-end (robustness against interferer, adjacent channels, and high linearity)
- The design of such systems is even more difficult due to

additional requirements like low power consumption and low costs. The efficient design of these mobile communication systems demands the use of state-of-the-art simulation tools.

A top-down design flow starts with the development of the system concept. System level simulators like CoCentric, SPW or Matlab allow to build an executable specification. The system level model comprises the DSP part of the system (e.g. modulation and coding), but the analog components (especially the RF front-end) are often neglected or idealized.

Complicated transmission techniques like high-speed WLAN need the common verification of analog and DSP components at an early design level. This paper demonstrates how the RF receiver front-end architecture can be evaluated within a WLAN system level simulation.

The work is incorporated in the German research project HGDAT, promoted by BMBF (01 M 3054). The Fraunhofer Institute has evaluated several simulation tools by means of system designs of Nokia. This includes actual design tools provided by the project partner Cadence.

2. The High-Speed WLAN System

Different transmission standards (ETSI, IEEE) exist for wireless LAN systems (table 1).

Approval	Standard	Freq. Band [GHz]	Data Rate [Mbps]
1997	802.11	2.4-2.4835	2, 1
1999	802.11a	5.15-5.35 5.725-5.825	54, 48, 36, 24, ..., 9, 6
1999	802.11b	2.4-2.4835	11, 5.5, 2, 1
2002 (expect.)	802.11g	2.4-2.4835	54, 48, ..., 6, 5.5, 2, 1

Table 1. IEEE WLAN standards

The task was to design a WLAN RF receiver module for the high-speed WLAN standard IEEE 802.11a, which operates at 5.2 GHz, using orthogonal frequency division multiplex (OFDM). The RF receiver amplifies and down-converts the received 5.2 GHz signal to the baseband. The demodulation and further synchronization is done in the

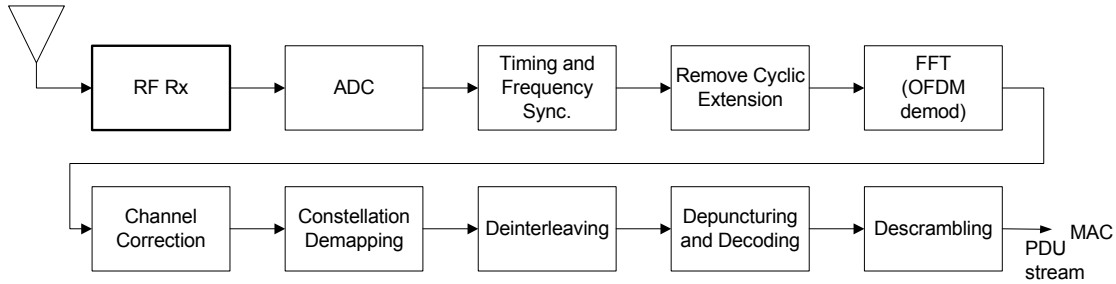


Figure 1. Block diagram WLAN receiver (physical layer)

digital signal processing (DSP) part of the receiver. The system architecture is outlined in this section.

2.1. IEEE 802.11a Transmission System (DSP)

The OFDM technique uses a number of modulated sub carriers for data transmission. Different digital modulation techniques can be used for the sub carriers according to the data rate. This distributes a high-rated data stream onto a set of sub carriers with a lower data rate.

IEEE 802.11a uses 48 data sub-carriers and 4 pilot carriers for the transmission. Figure 4 shows an OFDM signal at 5.2 GHz carrier frequency with an adjacent channel. The used modulation techniques are BPSK (at 6 Mbps), QPSK, QAM16 and QAM64 (at 54 Mbps).

The analog RF receiver subsystem down converts the received OFDM signal to the baseband. Many DSP procedures are necessary to decode the transmitted data:

- timing and frequency offset correction
- OFDM demodulation (using FFT)
- channel correction, constellation de-mapping (digital demodulation)
- deinterleaving, FEC decoding, descrambling

The decoded data stream is further processed in the MAC layer, which is not discussed in this paper.

2.2. Double Conversion Receiver (RF part)

The DSP part of the receiver has great complexity and realizes the most functionality which is necessary to properly decode OFDM signals. Nevertheless we need an analog RF subsystem which converts the RF OFDM signal down to the complex baseband. In that example it is done by a double conversion receiver shown in figure 2.

After signal amplification by a low-noise amplifier the signal is down converted at two mixer stages working at the same local oscillator (LO) frequency of 2.6 GHz. The first mixer converts the signal to half of the RF frequency, with a image frequency around zero. As there is no signal at 0 Hz, this architecture overcomes problems concerning image rejection. At the second mixer stage the RF input

signal and the LO signal both have the same frequency and therefore dc-problems caused by the self mixing products exist. DC-offsets and flicker (1/f) noise are filtered out by high-pass filtering between the stages. In the baseband section channel selection is done by low-pass filtering, suppressing the adjacent and non-adjacent channels. After filtering the signal is amplified by an automatic gain controlled amplifier (AGC).

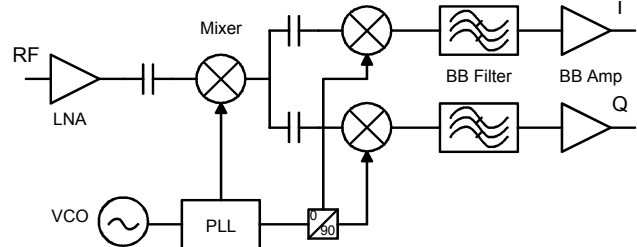


Figure 2. Double Conversion Receiver

The input signal of the receiver is in the range from -88 to -23 dBm for the wanted channel. The first adjacent channel may be 16 dBm, the second adjacent channel 32 dBm above this level. This requires high linearity, low noise and a good adjacent channel rejection.

3. Tools for the System Level Simulation

The requirements on the receiver and especially the RF part are high due to the sophisticated OFDM transmission technique. On the other hand the costs of the system and its design must be as low as possible. Simulation tools which allow the common verification of the DSP and the RF subsystems are needed to achieve these goals.

Cadence is a company, that provides CAD tools for different design tasks and design levels as well as interfaces between the tools. Due to the project partnership the tools were evaluated. The following tools are used to validate the RF receiver within the system environment:

- **Signal Processing Worksystem (SPW)** Release 4.8.1 System Level Simulator, DSP design
- **AMS Designer** Release 2.0 Mixed-Signal-Simulator (e.g. Verilog-AMS)
- **SpectreRF** (Spectre) Release IC 4.4.6 Analog Circuit Simulator with RF option

3.1. Signal Processing Worksystem

SPW allows to simulate complete transmission systems containing transmitter, channel and receiver. It is used in concept engineering, as modeling language C, C++ and SystemC are used. The simulator provides huge libraries with pre-defined models of typical components of telecommunication systems. Also reference models of telecommunication standards are available. Most of the provided models describe DSP algorithms.

The modeling accuracy for analog components (e.g. the RF subsystem) is restricted, because time discrete simulation algorithms are used to analyze the system. Nevertheless some effects of analog components can be represented in system level simulation. A library of common RF components (mixer, LNA, ...) is available. The co-simulation with the AMS designer can be used for a more accurate simulation of analog system parts.

The system description is entered via a block diagram editor. The simulator is controlled by a graphical user interface. A waveform viewer *SigCalc* and a filter design program is also provided.

SPW provides a model of a complete IEEE 802.11a transmission system, which performs a bit error rate (BER) measurement. It consists of transmitter, channel and receiver modules. The transmitter produces a standard compatible OFDM signal with a configurable data rate. The signal is transmitted over a channel model that can realize an additive white gaussian noise (AWGN) or a fading channel. The receiver model represents a complete receiver module including synchronization and channel estimation.

3.2. SpectreRF

Spectre is an analog simulation tool which can be used to simulate circuit level designs as well as analog behavioral models. The RF option *SpectreRF* provides specific simulation algorithms for the analysis and characterization of RF components. They allow an accurate analysis of noise and non-linearity, e.g. measurement of Compression Point, Intercept Points and Noise Figure.

For the simulation of the complete RF subsystem it is advisable to use behavioral models. They can be written in *Verilog-A*, the analog subset of *Verilog-AMS*. These models can be re-used later in the AMS-designer. The use of behavioral models will speed-up the simulation and allows the investigation of larger system parts. Behavioral models can also be used together with transistor level descriptions especially for the development of test-benches.

Like SPW, SpectreRF provides in the *rfLib* models of the mostly used components of RF sub-systems. The parameters of the models may differ from the parameters

of the corresponding SPW models.

SpectreRF is integrated in the Design Framework II (*DFII*). The system description can be entered as schematic or netlist. The simulations can run in interactive mode (analog artist) or in batch mode (e.g. controlled by *OCEAN* scripts).

3.3. AMS Designer

The Cadence AMS Designer enables the user to compile and simulate mixed signal HDL-source codes. The release 2.0 supports the mixed signal hardware description language Verilog-AMS, VHDL-AMS is announced. Verilog-AMS is a standard of the Open Verilog International subcommittee (OVI).

The Verilog-AMS language allows the reuse of Verilog (digital) and Verilog-A (analog) descriptions, but partially it is necessary to modify Verilog-A descriptions before they can be used with a Verilog-AMS simulator [4], [5].

The AMS Designer is used here for the co-simulation with SPW. It allows to use the analog behavioral models from the Spectre *rfLib*, which are coded in Verilog-A. Additionally SPICE built-ins and sub circuits can be also instantiated in a Verilog-AMS description.

Properties of the AMS Designer are:

- includes compiler, elaborator and simulator components, which can be started individually or together
- can be started in a batch- or interactive mode
- in the interactive mode the graphical user interface (GUI) allows to control the simulation, to probe signals and to set break points for debugging tasks
- signals can be displayed during the simulation runtime with the *signalscan* waveform viewer
- supports TCL (tool command language)-based commands for debugging tasks
- a Verilog Procedural Interface (VPI) enables to interact with another simulator

4. Simulation Flow and Experiences

The system is developed in a top-down design-flow. It is assumed, that an executable specification of the DSP subsystem exists in SPW. The RF system designer has specified the structure and main parameters of the RF subsystem. The following design steps are suggested:

- Creation of a hierarchical model of the RF part using the SPW RF models. Verification of the model within SPW simulation of the complete system.
- Model the RF subsystem in Spectre using the corresponding Verilog-A models. Verify the RF system separately using RF simulation techniques.

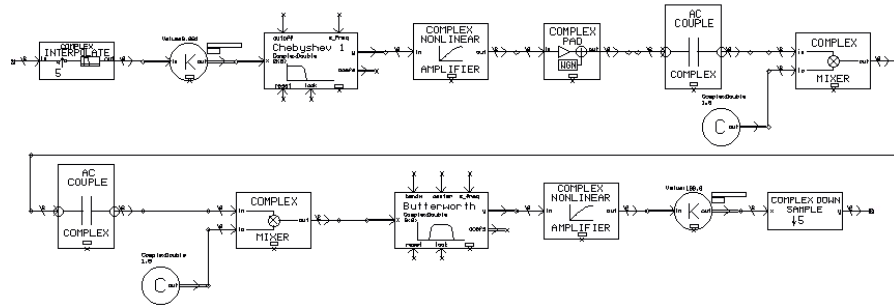


Figure 3. SPW schematic of the double conversion receiver

- Design the components of the RF subsystem (circuit level). Verification of the circuit designs in the RF subsystem model. Calibration of the behavioral models.
- Verification of the RF design in the DSP environment by generation of a Verilog-AMS netlist and co-simulation with SPW and AMS simulator.
- Other solution: Extraction of a black-box model of the complete RF subsystem in SpectreRF simulation which can be instantiated in SPW (J&K models, see [6])

The suggested design flow was evaluated with the WLAN example. The experiences are shown below.

4.1. SPW simulation standalone

The model of the RF part is created from models of the SPW *rfLib*. The library contains amplifier and mixer models. The filters are found in other SPW libraries. SPW provides models for complex baseband and passband signal representation. To achieve a sufficient simulation speed for bit error simulations the complex baseband models are used [7].

As a test-bench the IEEE 802.11a demo system is used, which is provided by SPW. The model provides the complete DSP algorithms of the physical layer of WLAN including transmitter, channel and receiver. The model of the double conversion receiver shown in figure 3 is inserted in front of the DSP receiver part. The input and output level of the RF subsystem must be adapted with constant multipliers.

The simulation manager allows to setup parameter sweeps. So it was possible to measure bit error rates versus critical parameters of the RF front-end, e.g. IP3 value of the LNA. Additionally an adjacent channel was added to the system. Therefore the transmitter model was duplicated and its OFDM signal was shifted by 20 MHz in the frequency domain. The baseband signal was over-sampled to fulfill the sampling theorem. The impact of the adjacent

channel to the BER is shown in figure 6.

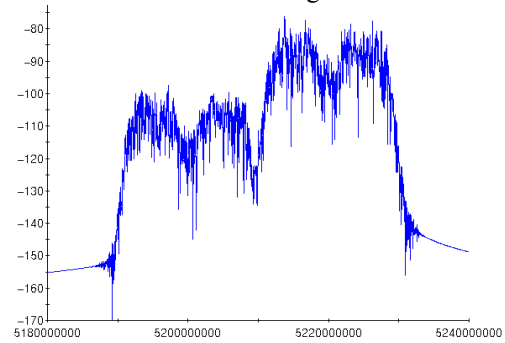


Figure 4. OFDM signal and adjacent channel

The simulation with SPW shows that the simulator is able to analyze very large systems in a sufficient time. It provides simulations in interpreted or compiled mode. The compiled mode (SPB-C) is suggested for long simulation times as necessary for BER computations.

4.2. SpectreRF simulation

The double conversion receiver architecture was modeled in Spectre with behavioral models of the corresponding library. Complex baseband and passband are available for typical RF building blocks. Unfortunately the model parameters from Spectre and SPW models are different in some cases.

While assembling the receiver by using baseband models from the Spectre *rfLib* it was recognized that no band-pass filter model is available which allows a bandwidth greater than 0.5 of the center frequency. A high- and a low pass filter was used instead.

The receiver model and its performance can be tested in SpectreRF in a transient simulation with OFDM signals. Other test benches with two tone signals allow in combination with the RF specific Periodic Steady State analysis several measurements of RF specific parameters. Details of the SpectreRF simulation are not explained here. The SpectreRF schematic of the double conversion receiver is the base for the co-simulation of the AMS designer and SPW.

4.3. SPW-AMS co-simulation

The IEEE802.11a transmission system is used again as test bench of the receiver. The double conversion receiver is now imported from a Verilog-AMS description. The following steps are necessary:

- the Verilog-AMS description is generated automatically by saving the Schematic in the DFII
- after few modifications the Verilog-AMS description is manually compiled by using the *ncvlog* compiler.
- from the netlist a SPW block can be generated by using the block wizard of SPW.
- now the block can be used in SPW system schematics
- for a co-simulation the simulator *SPW-AMS* has to be chosen in the SPW simulation manager
- after the simulation is started the simulation manager generates a C-file from the SPW schematic and imports the HDL from the work library. Afterwards the HDL description is simulated by the *AMS Designer* and the C-file from the SPW schematic will be simulated by the SPW *SPB-C* simulator.
- signals from the RF part can be displayed in the *signalscan* viewer, but the visualization capability for analog waveforms is restricted.
- if probes were set before simulating, the probed signals can be displayed by using the SPW *SigCalc* viewer

The simulation has shown, that the AMS Designer is a powerful tool and easy to use. In most cases a co-simulation with SPW runs without any problem, but under certain circumstances the AMS Designer causes problems.

A recognized problem is that the AMS designer does not support some functions for generating noise (*white_noise*, *flicker_noise*), which are widely used in behavioral models of RF blocks. These functions work only in small signal analyses, but the transient simulation of the AMS designer is a large signal analysis.

One work around is to include an additional noise source to the SPW part of the co-simulation. A more accurate solution is to insert a noise functionality to the analog models by using Verilog-AMS random functions. This solution is more difficult, since each RF sub-model contains separate noise sources, which must be modified. In doing so, it must be avoided that small and large signal noise functionality occur at the same time. Also it must be ensured, that the large signal noise shows the same behavior like the small signal noise function.

4.4. Accuracy of the used simulation methods

Analog solvers perform a continuous calculation of currents and node voltages in a circuit therefore the solutions

are very accurate. Whereas system level simulators work with equidistant samples and calculates signals instead of real currents and voltages. Thus system simulators deliver less accurate results than analog tools. The advantage is the good simulation performance of system simulators, which allows to analyze huge system parts.

So the SpectreRF simulation of the RF subsystem is more realistic than the solution of SPW, but SPW provides the performance for the common verification of RF and DSP subsystems. The accuracy can be increased by using improved models of the RF building blocks (including AM/PM conversion and impedance mismatch). The simulation results will be compared to measurements later.

5. Simulation Results

The performance of the transmission system can be evaluated by bit error rate (BER) or error vector magnitude (EVM) measurements.

5.1. BER measurement

The quality of a transmission system can be best determined by performing a bit error rate measurement. A BER enables to recognize the influence of parameter settings on the transmission result.

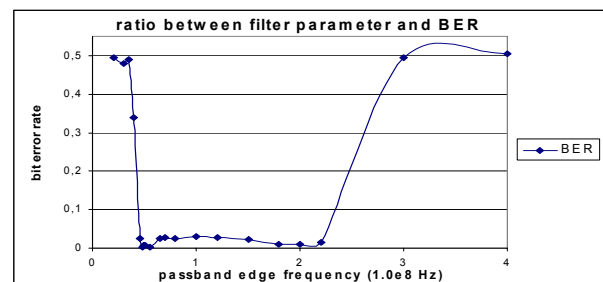


Figure 5. BER vs. filter bandwidth (with present adjacent channel)

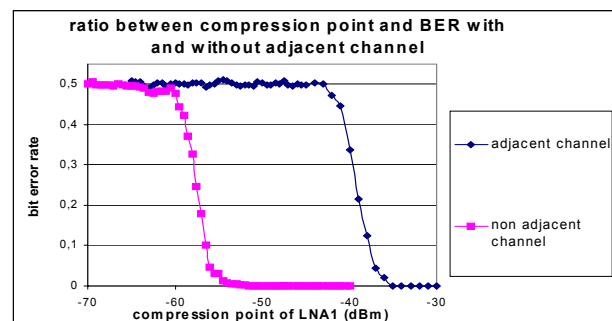


Figure 6. BER vs. compression point of first LNA

Bit error rate simulations of very complex systems like WLAN generate a large amount of simulation data. In order to avoid a data overload, it can be necessary to dese-

lect probes during simulations with a large number of samples or with multiple runs. In order to determine the influence of the RF subsystem on the transmission system the parameter input and output scale, compression point and third order intercept point were examined. Figure 5 shows the impact of the chebyshev filter bandwidth to the BER.

During a co-simulation it was not possible to examine the influence of the noise figure, because the AMS Designer does not support the Verilog-AMS noise functions. This causes, that the measured BER values were better than the results from the corresponding SPW only simulation.

5.2. EVM measurement

In contrast to a BER an error vector magnitude (EVM) describes the error rate of the really received OFDM symbols before they are estimated in the Viterbi decoder. The EVM measures the distance between the complex point of a received symbol to the ideal complex point of a reference.

An error vector magnitude (EVM) measurement was only performed while simulating a WLAN system which includes an ideal receiver model. The practical receiver model which includes channel estimation and synchronization is very complex. It was difficult to capture the received OFDM symbols from the internal receiver signals.

5.3. Simulation Time

The simulation time of the co-simulation is 30 to 40 times higher than the time of a pure SPW simulation, measured on a Sun Sparc Enterprise Server with 4 Ultra-4 processors shared in a network.

OFDM Packets	SPW simulation time [min]	Co-simulation time [min]
5	0.5	19
20	2.0	60
50	3.5	167

Table 2. Comparison of simulation time

6. Conclusion

Tools and models are available that allow the evaluation of a RF receiver architecture within the system environment. The impact of parameters of the analog subsystem to the system performance represented by the bit error rate could be shown.

The system level simulator SPW enables to simulate huge DSP systems such as the physical layer of a WLAN.

Analog system parts can be either modeled directly within SPW or they are integrated as co-simulation with the mixed-signal simulator AMS designer.

BER measurement gives the safest information about the system performance, because it comprises the complete signal path. Therefore large simulation times arise. To keep the simulation handy, it is mandatory to use complex baseband modeling technique in the RF system part.

During the system design the SPW simulation can be used to investigate the influence of architecture and parameters of the RF subsystem to the system performance. After that the RF subsystem can be further developed by using SpectreRF which provides RF specific analyses. For verification purpose it is possible to use the AMS simulator to include the RF design at different abstraction levels into the system level. Thereby it must be taken into account, that the performance of a co-simulation is lower than the performance of a pure SPW simulation, because co-simulation is more detailed.

SPW, SpectreRF and the AMS designer allow the verification of the RF subsystem at different levels of abstraction. The following points would improve the usability of the tools and their interfaces:

- make the SPW rLib more compatible to the SpectreRF models. The SpectreRF baseband models provide an extended functionality including AM/PM conversion, which must be realized in SPW by separate blocks
- availability of noise functions in the AMS designer, to ensure that the AMS simulation is compatible to SpectreRF simulations

Additionally the J&K models [6] are available to bring the RF subsystems of receiver and transmitter as black-box into a SPW system simulation.

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