DATE 2015 Best Paper Awards

Each year the Design, Automation and Test in Europe Conference presents awards to the authors of the best papers. The selection is performed by an award committee, based on the results of the reviewing process and the quality of the final paper.

D Track

**PHASENOC: TDM SCHEDULING AT THE VIRTUAL-CHANNEL LEVEL FOR EFFICIENT NETWORK TRAFFIC ISOLATION**

Anastasios Psarras\(^1\), Ioannis Seitanidis\(^1\), Chrysostomos Nicopoulos\(^2\) and Giorgos Dimitrakopoulos\(^3\)

\(^1\)Democritus University of Thrace, GR; \(^2\)University of Cyprus, CY

Visit Session ... [1]

A Track

**HARDWARE TROJAN DETECTION FOR GATE-LEVEL ICS USING SIGNAL CORRELATION BASED CLUSTERING**

Burcin Cakir and Sharad Malik, Princeton University, US

Visit Session ... [2]

T Track

**DIGITAL CIRCUITS RELIABILITY WITH IN-SITU MONITORS IN 28NM FULLY DEPLETED SOI**

Marine Saliva\(^1\), Florian Cacho\(^1\), Vincent Huant\(^1\), Xavier Federspiel\(^1\), Damien Angot\(^1\), Ahmed Benhassain\(^1\), Alain Bravaix\(^2\) and Lorena Anghel\(^3\)

\(^1\)STMicroelectronics, FR; \(^2\)IM2NP-ISEN, FR; \(^3\)TIMA, FR

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Best Paper Award Nominations

D Track

**ASYMMETRIC UNDERLAPPED FINFET BASED ROBUST SRAM DESIGN AT 7NM NODE**

Arun Goud Akkala, Rangharajan Venkatesan, Anand Raghunathan, Kaushik Roy

Purdue University

**FAST EYE DIAGRAM ANALYSIS FOR HIGH-SPEED CMOS CIRCUITS**

Seyed Nematollahi Ahmadyan, Shobha Vasudevan

University of Illinois at Urbana-Champaign

Eli Chiprout, Chenjie Gu, Suriyaprakash Natarajan

Intel

A Track

**WORKLOAD UNCERTAINTY CHARACTERIZATION AND ADAPTIVE FREQUENCY SCALING FOR ENERGY MINIMIZATION OF EMBEDDED SYSTEMS**

Anup Das, Akash Kumar, Bharadwaj Veeravalli, Rishad Shafik, Geoff Merrett, Bashir Al-Hashimi

University of Southampton, National University of Singapore

AN ULTRA-LOW POWER DUAL-MODE ECG MONITOR FOR HEALTHCARE AND WELLNESS

Daniele Bortolotti, Mauro Mangia, Andrea Bartolini, Riccardo Rovatti,
REDUCING TRACE SIZE IN MULTIMEDIA APPLICATIONS ENDURANCE TESTS
Serge Vladimir Emteu Tchagou, Alexandre Termier, Jean-François Méhaut, Brice Videau, Miguel Santana, René Quiniou
University of Grenoble Alpes, STMicroelectronics, University of Rennes, INRIA Rennes

GPU-ACCELERATED SMALL DELAY FAULT SIMULATION
Eric Schneider, Stefan Holst, Michael Kochte, Xiaoqing Wen, Hans-Joachim Wunderlich
University of Stuttgart, Kyushu Institute of Technology

EDAA Outstanding Dissertation Award 2014
Category “New Directions in Embedded System Design and Embedded Software”
Nan Guan, Ph.D.
New Techniques for Building Timing-Predictable Embedded Systems

Category “New Directions in Logic and System Design”
Zhenyu Sun, Ph.D.
High-Performance And Low-Power Magnetic Material Memory Based Cache Design

Category “New Directions in Physical Design, Design for Manufacturing and CAD for Analogue Circuits and MEMS”
Bei Yu, Ph.D.
Design for Manufacturing with Advanced Lithography

Category “New Directions in Logic and System Test”
Brandon Robert Noia, Ph.D.
Design-for-Test and Test Optimization Techniques for TSV-based 3D Stacked ICs

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