A Fully Digital Controlled Off-Chip $I_{DDQ}$ Measurement Unit

B. Straka, H. Manhaeve*, J. Vanneauville*, M. Svajda**

CEDO, Vidadeska 127, 61900 Brno, Czech Republic
Phone/Fax: +420 5 4321 4089, E-mail: straka@cedo.cz
* KHBO, Microelectronics Department, Zeeiijk 101, B-8400 Oostende, Belgium
Phone: +32 59 508996, Fax: +32 59 704215, E-mail: manhaeve@micro.khbo.be
** Technical University of Brno, Dept. of Microelectronics, Udolni 53, 602 00 Brno, Czech Republic
Phone: +420 5 41 211 690, Fax: +420 5 43 167 298, E-mail: svajda@umel.fee.vutbr.cz

Abstract

The paper describes a new Digital controlled Off-Chip $I_{DDQ}$ Measurement Unit (DOCMU), which provides reliable precision and relatively fast measurements, even with a high capacitive load, while the Device Under Test (DUT) is unaffected. The maximal resolution is 50nA and the accurate measurement range is 1mA. Unlike other $I_{DDQ}$ monitors, the DOCMU copes with external interference, as it needs no analogue pin to set the $I_{DDQ}$ limit and the noise at the $V_{DDQ}$ is eliminated via a special S/H feature. The DOCMU is also a testable $I_{DDQ}$ monitor, which is another unique feature.

Keywords:

$I_{DDQ}$, $I_{DDQ}$ monitors, testability, CMOS, integrated circuits, test hardware

1. Introduction

During the last decade, $I_{DDQ}$ testing is being recognised as an important additional test method in order to achieve better quality and reliability. It is well known that excessive quiescent supply current in CMOS ICs identifies a possible failure or a reliability problem. From the technical point of view, the main issue of $I_{DDQ}$ testing is the $I_{DDQ}$ measurement itself. The measurement is mostly done using dedicated circuits: $I_{DDQ}$ monitors/sensors. An $I_{DDQ}$ monitor is called an “on-chip monitor”, if the sensor is integrated together with the other circuitry, while “off-chip monitors” are inserted in the supply line outside the chip. Whether $I_{DDQ}$ is measured internally or externally, the normal operation of the DUT should not be affected by using a monitor. In addition, the monitor should be fast enough, reliable and accurate to be really applicable in an engineering/production testing environment. On-chip monitors are mostly simple structures. They are generally more sensitive and faster than off-chip monitors, because they are integrated on the chip and they do not drive any decoupling capacitance [1,3,4,12,20,21]. However supply voltage drop and extra delay must be considered in the design. On the other hand, off-chip monitors do not require extra silicon and pins, they are versatile and therefore preferred by IC producers.

The existing off-chip monitors [5,6,7,14,16,17] are mostly semidigital monitors. Some monitors ignore the essential decoupling rules [11,15,19] especially those based on the Keating-Meyer principle. The decoupling capacitor(s) must be placed very close to DUT’s supply pin(s). If any switch (relay, MOSFET) is inserted between supply pin and the capacitor, it will add a certain series resistance and inductance and the decoupling will loose its effect. Therefore, the decoupling capacitor(s) should be connected permanently to DUT’s supply pin(s) to really cover the transient peaks. Naturally, the decoupling capacitance present limits the speed of the $I_{DDQ}$ testing. However reliability and repeatability has a higher priority than speed in the production testing. The Industry reports that a few hundred/thousand test vectors are sufficient for a reasonable fault coverage even for large chips [18]. From this point of view, it seems useless to attempt speeds over 100kHz if proper decoupling is to be sacrificed.

It is not a real issue to design an $I_{DDQ}$ monitor, which works well in an ideal “laboratory” environment under exactly specified conditions. However, every monitor is a sensitive device and problems will occur as soon as it is put in noisy “industrial” environment. Hence a good monitor should be designed with regard to EMC, considering noisy/rippled supplies, interference etc. This requires new design approaches and techniques.
2. Description of the DOCLMU

2.1. General description of the DOCLMU

A new testable fully Digital Off-Chip IDD Measurement Unit (DOCLMU) was developed to measure the quiescent supply current of digital as well as analogue ICs. The DOCLMU was optimised to drive also heavy capacitive loads, which enables its use also for complex ASICs with multiple supply pins. The monitor provides IDD measurements at a relatively high test-speed, up to 30kHz. The DOCLMU exhibits a maximal resolution of 50nA. The operation of the DUT is not affected, as the monitor causes only a neglectable voltage drop (mV). The monitor is intended to be integrated in the test-head of standard automated test equipment (ATE), so it can be used to do IDD measurements of packed chips as well as of dies on wafers.

The DOCLMU belongs to the class of “fully digital monitors” according to the QTAG terminology, it also keeps back-compatibility with QTAG semidigital monitors [8,9,13]. Only digital ATE pins are needed to control all the functions of such a digital monitor, in contrast to semidigital monitors, which require also analogue ATE pin(s).

The DOCLMU is designed to be inserted between the VDD and the supply pin of DUT like an ordinary ampereter. The DUT is supplied from the VDD supply (provided by ATE) through the monitor. Such a configuration with common GND (ground) is mostly better than the configuration with a virtual ground because of the sensitivity for possible external interference and the availability of a hard reference.

The DOCLMU has 3 digital control pins (MODE, I/O, CLK), which interface to the ATE, 2 supply pins (+15V, -15V), and 2 IDD current-path pins (VDD, DUT) as shown in figure 1. MODE is an asynchronous digital input controlling the measurement cycle. I/O is a bi-directional pin, which acts as data output or data input clocked by the CLK pin with a maximal frequency of 10MHz. The DOCLMU also provides 1 analogue input (V_PASS/FAIL), 1 analogue output (VDDO) to keep it compatible with semidigital monitors. These 2 analogue pins are optional and they are normally not used, since the DOCLMU can be fully controlled via the digital pins. Another optional pin, the digital data input (DI) can be used for chaining several monitors together.

The DOCLMU consist of 2 separated shielded boxes placed on a PCB, one with the sense part (Sense Unit, Bypass, S/H, Compensation, Over-current, Input Digital Potentiometer and Calibrator) and the other one with the control part (Output Filter, Comparator, 16-bit D/A, 16-bit A/D with the Switch and the Control Unit). The main purpose of the sense part is to measure the IDD so that the ATE can read the results or it can configure the monitor via the control part.

The Sense Unit converts the IDD current accurately to a corresponding VDDO voltage with a ratio 500mV per μA. Semidigital monitors are often suffering from electromagnetic interference (EMI), as the VPF limit is set externally using an analogue ATE pin. In addition, the analogue outputs of some testers have a poor resolution, which further degrades the performance of a semidigital monitor. The DOCLMU solves both issues, using a precision serial D/A converter, which generates the internal pass/fail voltage level with a resolution of 76μV (15nA). The Output Filter limits the bandwidth, which decreases the noise level. The measured VDDO is compared with the VPF limit by the Comparator, resulting in the pass/fail flag.

![Figure 1. Block schematic of the DOCLMU.](image)

The monitor uses a high speed precision serial 16-bit A/D converter (10μs conversion time), which enables to measure the exact IDD value in one measurement cycle. The ATE can also perform a binary search procedure based on using the D/A and the pass/fail flag. This is more...
accurate, but it takes multiple measurement cycles until exact $I_{DDQ}$ value is found.

All the control logic is implemented in a single component - a high density Programmable Logic Device (PLD). The use of a PLD with in-system programmability provides excellent flexibility as it can be reprogrammed directly on the board, without removing the PLD from the socket. The PLD also saves space, improves and simplifies the PCB and lowers the radiation.

The configuration of the monitor is stored in a 24-bit shift register controlled by the ATE. This register drives analogue switches, which select the monitor's working configuration. 8-bits select the Input Resistance of the DOCIMU and 4-bits determine the cut-off frequency of the Output Filter. As a result, the ATE can optimise the DOCIMU for a wide range of loading capacitance and measurement speeds.

The A/D converter can not only be used to measure the $V_{DDQ}$ voltage, but also the output voltage of D/A, the $V_{PP}$ voltage, the actual voltage at the DUT terminal etc. This is a very important feature, as it makes the monitor testable and the ATE can verify, if the monitor works properly. The Analogue Switch at the input of the converter occupies 4 bits from the configuration shift register.

The Calibrator of the DOCIMU offers a set of calibration resistors (up to 8-bits), which serve the ATE to check and to calibrate the offset and the gain error, when an accurate measurement is required.

2.2. The DOCIMU operation.

A new measurement cycle is initiated by the ATE by placing the monitor in bypass mode and holding MODE pin 'high' while a new test vector is applied to the DUT, as illustrated in figure 2.

During this mode the Bypass switch is turned on to bypass the (high) transient current drawn by DUT. The Bypass Unit together with the decoupling capacitor $C_L$ ensures that the operation of the DUT is not affected during this critical period. The MODE pin not only controls the Bypass, but also the direction of the I/O pin. In bypass mode, the I/O pin acts as a serial data input, enabling the ATE to load the 16-bit D/A ($I_{DDQ}$ limit) and the 24-bit configuration shift register.

When the MODE signal is 'low', the monitor is placed in measurement mode, I/O becomes an output and the Bypass switch is turned off. At the end of the measurement cycle, $V_{DDQ}$ is settled and the ATE can read a valid pass/fail flag via the I/O pin or it can start the A/D conversion. The I/O pin is 'low' (fail), if the measured $I_{DDQ}$ exceeds the $I_{DDQ}$ limit determined by VP/F, otherwise I/O is 'high' (pass).

2.3. New features of the DOCIMU

The Performance of the monitor depends mainly on the Sense Unit. The sense opamp converts the $I_{DDQ}$ to a $V_{DDQ}$ voltage via a feedback resistor $R_S$, while the voltage at its inverting input is following $V_{DDQ}$, due to the regulating loop, as shown in figure 3.

![Figure 3. Bypass compensation and SH feature](image)

The variable input resistor $R_{IN}$ determines the pulse response and limits the noise gain. A too low input resistance results in damped oscillations and excessive output noise, while a too high input resistance makes a voltage drop and slows down the pulse response. A high loading capacitance $C_L$ requires a low $R_{IN}$ and vice versa. $R_{IN}$ is typically 5Ω to 100kΩ for $C_L$ ranging from 2μF to 100nF. The voltage across the sense resistor $R_S$ is
further amplified by the instrumentation amplifier. \( V_{\text{IDDQ}} \) is derived from the \( I_{\text{IDDQ}} \) using a conversion ratio of 5mV/\( \mu \text{A} \), since \( R_s = 1 \text{k} \Omega \) and the amplification factor is set to 5.

\( I_{\text{IDDQ}} \) monitors usually use a MOSFET switch to bypass the high transient \( I_{\text{DD}} \). However every MOSFET has parasitic capacitors \( C_{gs} \) and \( C_{gd} \), which are important, as they can have a value of a few nF for low \( R_{on} \) MOSFETs. The resulting charge injection when the MOSFET is switched on causes the peak at the end of the bypass mode (fig. 2). The settling takes time and prolongs the measurement period. On-chip methods [2], to compensate the switch, cannot be applied in designs with discrete components, as single components have a much higher dispersion of parameters than matched on-chip components. However, the DOCIMU is equipped with an auxiliary circuit, which reduces the peaks approximately 5 to 10 times in comparison with uncompensated bypass switch and therefore the settling is improved about 2 time-constants \( R_sC_{gs} \), as illustrated in figure 4. Both compensation bipolar transistors require no matching and they can also be replaced by MOSFETs with low parasitics. The BYPASS control signal is derived from the MODE signal, using an optocoupler.

![Figure 4. Detail of the settling.](image)

Traditional voltage based testing of digital ICs obviously does not require a high quality \( V_{\text{DD}} \) supply. However, a noisy \( V_{\text{DD}} \) reference makes a noisy \( I_{\text{IDDQ}} \), so \( I_{\text{IDDQ}} \) testing is affected naturally. The \( V_{\text{DD}} \) power supply provided by the ATE is too noisy for precision \( I_{\text{IDDQ}} \) measurements, as its spectrum exhibits a line ripple (50Hz), switching noise, thermal noise etc. This causes a problem, as the \( V_{\text{DD}} \) noise cannot be filtered simply without prolonging the \( V_{\text{DD}} \) reaction time. In engineering / production testing, it can be desired to measure the \( I_{\text{IDDQ}} \) for different \( V_{\text{DD}} \) voltages. In addition the \( V_{\text{DD}} \) is set to zero whenever the DUT is removed or placed in the test fixture not to damage the DUT. Therefore, an \( I_{\text{IDDQ}} \) monitor should settle and be ready to measure within a reasonable period (a few ms) after a \( V_{\text{DD}} \) change occurs. The existing \( I_{\text{IDDQ}} \) monitors either ignore the \( V_{\text{DD}} \) noise or place a capacitor between \( V_{\text{DD}} \) and ground. Since the internal resistance of \( V_{\text{DD}} \) power supply is very low, this simple RC low-pass does not cut off the AF noise.

The DOCIMU is equipped with a special double sample/hold feature to reject \( V_{\text{DD}} \) noise & ripple. The used principle is relatively simple, but extremely efficient. Actually there are two \( S/H \) circuits in the DOCIMU (fig. 3). Normally the Bypass MOSFET is considered only as a bypass switch, but in reality it is a sample switch and the decoupling capacitor \( C_I \) acts as a hold capacitor. If also a \( S/H \) is added to the noninverting input of the sense opamp, then the DOCIMU achieves an excellent \( V_{\text{DD}} \) noise rejection ratio. This unique approach is based on fact that instant value of any AF noise, ripple or interference, which modulates the \( V_{\text{DD}} \), is sampled during bypass mode and held in the measurement mode. The essential thing is that there is exactly the same instant value of the \( V_{\text{DD}} \) voltage at both the opamp's inputs, as the samples are taken at the same time. The matching of both \( S/H \) circuits is not critical at all, but both MOSFETs should be capable to charge their hold capacitors in period shorter than 10\( \mu \)s in order to cover whole AF spectrum <1kHz. Elimination of the \( V_{\text{DD}} \) noise is possible using the \( S/H \) feature, as the \( I_{\text{IDDQ}} \) monitor is basically a band pass. Its DC gain is 1 (follower) from \( V_{\text{DD}} \) point of view, then the gain is growing with frequency due to decreasing impedance of \( C_I \), and finally the gain is falling down at high frequencies due to the opamp's gain bandwidth. The double \( S/H \) feature enables to separate the \( V_{\text{DD}} \) noise, which would be normally highly amplified, from the DC based \( I_{\text{IDDQ}} \) measurement.

### 2.4. DOCIMU specifications

- 2 supply pins, 2 current measurement pins, 3 digital interface pins (CMOS/TTL level)
- Test speeds: from 35\( \mu \)s to 500\( \mu \)s (30kHz to 2kHz)
- Range of the loading capacitance \( C_I \): 100nF - 2\( \mu \)F
- Measurement range: 0 - 1000\( \mu \)A
- I/V conversion ratio: 5.00nmV/\( \mu \)A
- Resolution: 50nA - 1\( \mu \)A
- Total accuracy: resolution+0.2% from the value
- Range of DUT's \( V_{\text{DD}} \): 1V - 8V
- Monitor's supply voltage: symmetrical+15V/-15V
- Max. transient current \( I_{\text{IDDQ}} \): 10A
- Internal resistance in bypass mode: <0.05\( \Omega \)
- Internal resistance in measurement mode: 2.5\( \Omega \) - 100\( \Omega \) (according to the configuration)
- Size of the monitor: 22cm x 8cm x 2cm
3. Measurement results and verification

The DOCIMU, as shown in figure 5, is expected to replace its semidigital predecessors (OCIMU and POCIMU), which are successfully used by Alcatel-Bell and Alcatel-Mietec in Belgium for engineering and production in IDDQ testing already for several years. In order to evaluate monitor's accuracy exactly, a set of well known resistors was used instead of ICs. The absolute error (i.e., resolution) ΔVDD is determined by peak-to-peak value of the output noise, which is growing with the loading capacitance CL and the measuring frequency f, as shown in figure 6.

The measurements also confirmed a very high VDD noise rejection. A sine waveform was modulated on supply VDD=5.000V and swept to emulate properly the external noise/ripple/interference. A 10mV magnitude caused a drastic degradation of the resolution, if only traditional RC low-pass filter was used. On the other hand, the new DOCIMU with the double S/H feature, exhibits no or neglectable resolution degradation under the same test conditions. The double S/H improves the resolution approximately 100 times when high level AC signals are modulated on the VDD. The S/H exhibits the high rejection in the whole AF range, while the spectrum above 10kHz is cut-off by the filtering capacitor Cf. Other measurements showed that the DOCIMU reacts very quickly to VDD changes - 100μs is sufficient to sample the new VDD value.

Table 1 shows a comparison of the basic parameters of existing off-chip IDDQ monitors including the DOCIMU.

<table>
<thead>
<tr>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>Developed by</td>
<td>Sandia Labs USA</td>
<td>Advantest Japan</td>
<td>Megatest USA</td>
<td>Philips Holland</td>
<td>U.BIST group Slovak/Belgium</td>
<td>U.BIST group Czech/Belgium</td>
<td>U.BIST/A/Alcatel Czech/Belgium</td>
</tr>
<tr>
<td>Implementation</td>
<td>discrete</td>
<td>discrete</td>
<td>discrete</td>
<td>CMOS 0.8</td>
<td>CMOS 0.7</td>
<td>BiCMOS 2um</td>
<td>discrete</td>
</tr>
<tr>
<td>measurement principle</td>
<td>Keating-Meyer</td>
<td>opamp/IV converter</td>
<td>opamp/IV converter</td>
<td>current mirror</td>
<td>CCH Current Conveyor</td>
<td>opamp/IV converter</td>
<td>opamp/IV converter</td>
</tr>
<tr>
<td>Max. speed f'</td>
<td>250kHz</td>
<td>1MHz</td>
<td>10kHz</td>
<td>50kHz</td>
<td>50kHz</td>
<td>2MHz</td>
<td>20kHz</td>
</tr>
<tr>
<td>Max. f' at CL=100nF</td>
<td>10kHz</td>
<td>50kHz</td>
<td>50kHz</td>
<td>50kHz</td>
<td>30kHz</td>
<td>20kHz</td>
<td>30kHz</td>
</tr>
<tr>
<td>Max. resolution resol. at CL=100nF</td>
<td>~ 500μA</td>
<td>~ 1μA</td>
<td>10nA</td>
<td>~ 30nA</td>
<td>10nA</td>
<td>500pA</td>
<td>200nA</td>
</tr>
<tr>
<td>Accuracy at 10nA</td>
<td>~ 5%</td>
<td>~ 20%</td>
<td>~ 3%</td>
<td>~ 3%</td>
<td>~ 1%</td>
<td>~ 1%</td>
<td>~ 1%</td>
</tr>
<tr>
<td>Output value via</td>
<td>8 bit A/D</td>
<td>A/D</td>
<td>A/D</td>
<td>pass/fail flag</td>
<td>pass/fail flag</td>
<td>pass/fail flag</td>
<td>16bit A/D, pass/fail flag, 16 bit D/A</td>
</tr>
<tr>
<td>VDD variation</td>
<td>high</td>
<td>1V</td>
<td>0.7V</td>
<td>300mV</td>
<td>~ 200mV</td>
<td>&lt;100mV</td>
<td>&lt;100mV</td>
</tr>
<tr>
<td>I/O control pins</td>
<td>~ 3</td>
<td>4</td>
<td>3</td>
<td>3</td>
<td>3</td>
<td>3</td>
<td>3</td>
</tr>
<tr>
<td>Other interesting features</td>
<td>high speed at low CL</td>
<td>high speed current source</td>
<td>wide range</td>
<td>small size</td>
<td>small size, optimised as on-chip monitor</td>
<td>small size, integrated 0.5Ω bypass</td>
<td>EMI immunity, testability, wide IDDQ range</td>
</tr>
</tbody>
</table>

Table 1. Off-chip IDDQ monitors - review
4. Conclusions

A new Digital Off-Chip $I_{DDQ}$ Measurement Unit is presented. The main advantage of this unit is a relatively high accuracy in wide measurement range at reasonable speed, while the circuit under test is unaffected by the $I_{DDQ}$ testing. The DOCIMU is a testable monitor, it exhibits a high EMI immunity, due to the digital control, the double S/H feature and the special shielding. The unit is versatile, flexible and it provides a cost effective $I_{DDQ}$ measurements and is applicable to a wide range of digital as well as analogue ICs.

In the future the DOCIMU will be probably implemented in silicon via extension of the I/OIMU circuit. All existing integrated $I_{DDQ}$ monitors are semidigital. Therefore, it is expected that the integrated DOCIMU will overcome them in versatility and EMI immunity.

Acknowledgements

This work was supported partly by the EC in the frame of the COPERNICUS project UBISTA (ref: COP94-0391) and partly by Alcatel-Bell and Alcatel-Mietec. The OCIMU monitor and its operating principle are patented by Alcatel.

References