



Call for Participation



DATE 2010 Friday Workshop on

3D Integration

— Applications, Technology, Architecture, Design, Automation, and Test —

Dresden, Germany

Friday March 12, 2010

<http://www.date-conference.com/conference/date10-workshop-W5>

The **Design, Automation, and Test in Europe** conference and exhibition is the main European event bringing together designers and design automation users, researchers and vendors, as well as specialists in hardware and software design, test and manufacturing of electronic circuits and systems. The conference includes plenary invited papers, regular papers, panels, hot-topic sessions, tutorials and workshops, two special focus days, and a track for executives. **Friday Workshops** are focusing on emerging research and application topics. At DATE 2010, one of the Friday Workshops is devoted to **3D Integration**. This one-day event consists of two invited keynote addresses, regular and poster presentations, and a panel session.

WORKSHOP DESCRIPTION

3D Integration is a promising technology for extending Moore's momentum in the next decennium, offering heterogeneous technology integration, higher transistor density, faster interconnects, and potentially lower cost and time-to-market. But in order to produce 3D chips, new capabilities are needed: process technology, architectures, design methods and tools, and manufacturing test solutions. The goal of this Workshop is to bring together researchers, practitioners, and others interested in this exciting and rapidly evolving field, in order to update each other on the latest state-of-the-art, exchange ideas, and discuss future challenges. The first edition of this workshop took place in conjunction with DATE 2009 (see <http://www.date-conference.com/conference/date09-workshop-W5>).

WORKSHOP PROGRAM

The workshop program contains the following elements.

- Two invited keynote addresses
 - "What We Have Learned from SOC Is What Is Driving 3D Integration"
by Cheng-Wen Wu (ICL/ITRI and National Tsing-Hua University, Taiwan)
 - "OSAT – Role as Partner in 3D Integration"
by ChoonHeung Lee (Amkor Technology, Korea)
- Two sessions with in total six regular presentations
- Two poster sessions
- A panel session

For the detailed version of the program, please turn over.

PARTICIPATION and REGISTRATION

You are invited to participate in the workshop. Participation requires registration and a registration fee. Registration will be available through the DATE'10 web site, as well as on-site in Dresden, Germany. Check the DATE web site (<http://www.date-conference.com>) for rates and other information. Workshop registration includes luncheon, coffee breaks, and download access to the Electronic Workshop Digest, containing extended abstracts, papers, slides, posters.

MORE INFORMATION

<http://www.date-conference.com/conference/date10-workshop-W5>

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08:30h: SESSION 1: OPENING

Moderator: Peter Schneider – Fraunhofer Institute, DE

08:30h: Welcome Address

08:50h: **Keynote Address:**

What We Have Learned From SOC Is What Is Driving 3D Integration
Cheng-Wen Wu – ICL, ITRI, TW / National Tsing-Hua Univ., TW

One of the most serious issues that IC developers face today is the development cost of a typical system-on-chip (SOC) using state-of-the-art technology – tens of million dollars for a case, and the cost continues to soar with the ever innovating technology. Today, more and more people are looking for alternative solutions, and three-dimensional (3D) integration is a feasible one that provides better or equal performance with lower cost, especially the development cost. Stacking dies using the Through-Silicon-Via (TSV) technology has been considered one of the most promising solutions to extending the life of Moore's Law in semiconductor industry, but of course there are problems to be solved before the infrastructure can be set up to support the industry for manufacturing TSV-based 3D integrated devices. In this talk we will discuss the design and test issues, and possible solutions for 3D integrated devices. Specifically, stacked dies will face the severe problem of exponential decay rate in their quality if the currently employed post-bond testing is not changed. We will propose a practical test methodology for wafer-on-wafer and die-on-wafer 3D integration, which is a solution extended from our SOC test methodology. Our approach allows die test before bonding, TSV test for vertical interconnect verification, as well as die test in all layers of the stack after bonding.

09:25h: **Keynote Address:**

OSAT – Role as Partner in 3D Integration
ChoonHeung Lee – Amkor Technology, KR

Outsourced semiconductor assembly and test (OSAT) providers have developed and scaled up new technologies for 3D integration over the past decade to become a strategic partner to semiconductor suppliers across the globe. OSAT capabilities have been critical to the industry in delivering the billions of stacked die and stacked package technologies that have been critical components for a wide range of mobile and high-performance applications to date. Now OSAT providers are working closely with their semiconductor suppliers to develop the technologies and capacities required to support a wide range of new 3D integration requirements utilizing TSV interconnects and flip-chip on flip-chip stacked structures. This talk will summarize various TSV supply chain flows and technologies OSAT providers are developing in partnership with customers, outline the critical TSV wafer processing and package assembly requirements OSAT providers must support, and summarize the TSV technology development status within OSAT industry leader Amkor Technology.

10:00h: SESSION 2: POSTERS

Posters (see right) - coffee + tea break

10:30h: SESSION 3: PAPERS

Moderator: Herb Reiter – Eda2Asic, USA

10:30h: 3D-PIC: An Error-Tolerant 3D CMOS Imager,
Hsiu-Ming (Sherman) Chang, Kwang-Ting (Tim) Cheng – UC Santa Barbara, USA; Jiun-Lang Huang – Natl. Taiwan Univ., TW; Ding-Ming Kwai – ITRI, TW; Cheng-Wen Wu – ITRI, TW / Natl. Tsing-Hua Univ., TW

11:00h: An Analytical Study on the Role of Thermal TSVs in a 3D-IC Chip Stack,
Min Ni, Qing Su, Zongwu Tang, Jamil Kawa – Synopsys, USA

11:30h: A Novel NOC Architecture Framework for 3D Chip MPSoC Implementations,
Konstantinos Tatas, Costas Kyriacou – Frederick Univ., Cyprus; Alexandros Bartzas, Kostas Siozios, Dimitrios Soudris – Natl. Techn. Univ. of Athens, GR

12:00h: LUNCHEON BREAK

13:00h: SESSION 4: PAPERS

Moderator: Stojan Kanev – Cascade Microtech, DE

13:00h: High Aspect-Ratio Through-Silicon Vias: How Molecular Engineering Impacts the 3D-IC Design Space,
Claudio Truzzi, Frederic Raynal, Vincent Mevellec – Alchimer, FR

13:30h: Debonding of Temporary Bonded Wafers with Topography for 3D Integration,
Peter Bisson, Sumant Sood, Jim Hermanowski, Wilfried Bair – Süss MicroTec, USA

14:00h: Modeling TSV Open Defects in Three-Dimensional Memory,
Li Jiang, Yuxi Liu, Qiang Xu – Chinese Univ. of Hong-Kong, HK

14:30h: SESSION 5: POSTERS

Posters (see right) - coffee + tea break

15:00h: SESSION 6: PANEL DISCUSSION

“3D: A Reality?”

Moderator: Jean-Christophe Eloy – Yole Développement, FR

Panelists: Rob Aitken – ARM, USA
Eric Cirot – ST-Ericsson, FR
Stefan Gasteiger – Advantest, DE
Vassilios Gerousis – Cadence Design Systems, USA
Rajiv Maheshwary – Synopsys, USA
Jochen Reisinger – Infineon Technologies, DE

16:00h: CLOSURE

POSTER SESSIONS 2 and 5

10:00-10:30h and 14:30-15:00h

1. Repeater Insertion Techniques for 3D Interconnects,
Hu Xu, Vasilis Pavlidis, Giovanni De Micheli – EPFL, CH
2. Partitioning Methods for Unicast/Multicast Routings in 3D Mesh NOCs,
Masoumeh Ebrahimi, Masoud Daneshmand, Pasi Liljeberg, Hannu Tenhunen – Univ. of Turku, FIN
3. Routing Strategies and Algorithms for Interposer-Based 3D Stacks,
Andy Heinig – Fraunhofer Inst. for ICs, DE
4. Measurement and Efficient Modeling of the RF Behavior of Interconnect Structures in 3D Systems,
Jörn Stolle, Sven Reitz, Peter Schneider, Steffen Prusseit – Fraunhofer Inst. for ICs, DE; Florian Schmitt, Horst Röhm – NXP Semiconductors, DE; Maciej Wojnowski – Infineon Technologies - DE
5. Practical 3D Tool Flow: 3D Placement and LVS,
Thorlindur Thorolfsson, Nariman Moezzi-Madani, Paul Franzon – North-Carolina State Univ., USA
6. A Novel Interlayer Bus Architecture for Three-Dimensional Network-on-Chips,
Masoud Daneshmand, Masoumeh Ebrahimi, Pasi Liljeberg, Hannu Tenhunen – Univ. of Turku, FIN
7. New Developments in High-Throughput Scanning Acoustic Microscopy for Automated Inspection of Bonded Wafers,
Peter Czurratis, Peter Hoffrogge – PVA TePla Analytical Systems, DE
8. New Circuit and Electro-Magnetic Simulation System for 3D LSI,
Hideyuki Aoki, Shigenori Otake, Tomokazu Mizukusa – ASET, JP; Hideki Asai – Shizuoka Univ. JP; Masahiko Arikawa, Yasuo Shimizu, Kazuo Kato – ASET, JP
9. Development of Layout and Physical Verification Flow for 3D IC Design,
Jing Jou Tang – ITRI, TW / Southern Taiwan Univ. TW; Jan Liang Wu – Southern Taiwan Univ., TW / Himax Technologies, TW
10. 3D Integration with TSV Interconnects,
Jérôme Baron, Jean-Christophe Eloy – Yole Développement, FR
11. Power Integrity of 3D Integrated Chips,
Waqar Ahmad, Hannu Tenhunen – KTH, SE
12. Design of an Efficient Hierarchical Router for Large 3D NOCs,
Walid Lafi, Didier Lattard, Ahmed Jerraya – CEA-LETI, FR
13. RF NOC: A New Paradigm for Very Large Scale Three-Dimensional On-Chip Interconnect Networks,
Alexander Wei Yin – Univ. of Turku, FIN; Gangming Lv – Xi'an Jiaotong Univ., CN; Cheng Tao, Pasi Liljeberg, Hannu Tenhunen – Univ. of Turku, FIN
14. An Asynchronous Serial Link for a 3D Network-on-Chip,
Florian Darve, Pascal Vivet – CEA-LETI, FR
15. Thermal Modeling and Experimental Validation of Thermal Effects of 3D-ICs,
Adi Srinivasan, Edmund Cheng – Gradient Design Automation, USA; Herman Oprins, Geert Van der Plas – IMEC, BE
16. 3D IC Test Challenges and Probing Concepts,
Stojan Kanev, Thomas Thäringen Jörg Kiesewetter – Cascade Microtech, DE; Erik Jan Marinissen, Luc Dupas – IMEC, BE
17. Plan, Implement and Analyze: 3DIC with Through-Silicon Vias,
Vassilios Gerousis – Cadence Design Systems, USA; and partners from ST Microelectronics, IMEC, and Qualcomm
18. Cost-Effectiveness of Wafer-to-Wafer 3D Chip Stacking with Matching Pre-Tested Wafers,
Jouke Verbree – Delft University of Technology, NL; Erik Jan Marinissen, Philippe Roussel, Dimitrios Velenis – IMEC, BE
19. Role of Leveler for ECD Copper Filling of TSVs,
D. Rohde, C. Jäger, N. Töteberg, A. Uhlig, T. Beck – Atotech Deutschland, DE
20. Investigation on Mechanical Stress Influence on MOS Transistor Parameter Fluctuation in 3D Heterogeneous Devices,
Grzegorz Janczyk, Tomasz Bieniek, Jerzy Szytnka, Piotr Grabiec – Inst. of Electron Technology, PL
21. Methods and Tools for 3D Heterogeneous Design,
Felipe Frantz, Lioua Labrak, Ian O'Connor – Université de Lyon, FR
22. Holographic Photolithography for 3D Integration,
Gavin Williams, Jesus Toriz-García, Luke Seed – University of Sheffield, UK; Richard McWilliam, Alan Purvis – Durham University, UK; Peter Ivey – Innotech, UK
23. Vision Sensor with a SIMD Processor Array in a Vertically Stacked 3D Integrated Circuit Technology,
Piotr Dudek, Alexey Lopich – University of Manchester, UK; Viktor Gruiev – Washington University in St. Louis, USA

Other 3D Integration Activities during DATE Week

- Monday March 8, 09:30-18:00h
DATE Full-Day Tutorial (requires separate registration via DATE)
'Chip-Package Co-Design Challenges for 3D Integration'
- Thursday March 11, 16:00-17:30h
DATE'10 Conference Hot-Topic Session 12.2 (requires DATE registration)
'3D Stacked ICs: Technology, Design, and Test'
- Thursday March 11, 18:00-21:00h
Global Semiconductor Alliance – EDA Interest Group Meeting
'3D/TSV Technology'
Organizer: Herb Reiter – eda2asic, USA