

ID: 21

Research Institute: National Chung Cheng University

Presenter: Jih-Sheng Shen, Pao-Ann Hsiung

Demonstrator name: PRESSNoC

Title: Power-Aware and Reliable Encoding Schemes Supported Reconfigurable Network-on-Chip Architecture

Due to advanced process technologies on one hand, the decreasing distance between wires has led to significant crosstalk interferences among adjacent wires; while on the other hand, the ratio of wire to gate power consumption has increased significantly such that the power consumed by wires can no longer be neglected in any power estimation model. These two problems have become very severe in a Network-on-Chip (NoC) because of the large number of wires used for parallel communication. Further, the applications communicating via an NoC and the NoC itself may both have varying run-time requirements on reliability and power-efficiency. To meet application-specific and platform-specific requirements dynamically, a *Power-aware and Reliable Encoding Schemes Supported reconfigurable Network-on-Chip* (PRESSNoC) architecture is proposed, which allows processing elements, routers, and data encoding methods to be selected and reconfigured at run-time instead of pre-integrating all encoding strategies into an NoC at design time. Further, an intelligent selection of encoding methods is achieved through a *REasoning And Learning* (REAL) framework that can dynamically investigate the tradeoffs among reliability requirements, power reduction requirements, performance overhead, and hardware resource utilization. We implemented an instance of PRESSNoC on a Xilinx Virtex 4 FPGA device, which required 25.5% lesser number of slices compared to a conventional NoC with full-fledged encoding methods. The average benefit to overhead ratio of the PRESSNoC is greater than that of a conventional NoC by 71%, 32%, and 277%, when we consider the individual effects of interference rate per instruction, application domains, and system characteristics, respectively. From a cross analysis among the three different considerations, we found that 81% of the benchmark applications required different encoding strategies to meet different requirements. It not only demonstrates the need for a dynamically reconfigurable NoC that supports hardware encoding strategies selection at run-time for each individual application, but also shows that PRESSNoC induces a higher probability toward the reduction of crosstalk interferences and dynamic power consumption, at the same overheads of performance and hardware usage.