A Solution to optimize shared Memory BIST systems

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More and more complex functionalities are currently implemented inside SoC which leads to embed hundreds of memories having different sizes and properties. Testing these memories has consequently become a key challenge. On-chip testing using memory BIST is an efficient solution in terms of test time and time to market [1, 2]. As a result, academic and industrial communities are increasingly focusing on memory BIST.

For memory BIST insertion, a trade-off between area, test peak power and test time has to be considered which leads to share memory BIST logic [3, 4]. Indeed having dedicated BIST blocks for each memory would mean an unacceptable area overhead. Besides sharing memory BIST logic helps optimizing power consumption and test time. In this framework, the objective is to obtain an optimal solution for memory BIST sharing respecting all associated constraints.

Our sharing memory BIST approach considers the whole set of memories in a chip. In this context, the BIST system is composed of a set of collars. The collar executes tests on the memory and reports status on memory test execution. In addition to the dedicated approach, which consists in associating one collar to each memory, a collar can also be shared between memories either in sequence or in parallel. Parallel collars help reducing test time, while sequential collars help reducing power consumption. Both types of shared collar also reduce area.

Our research aim is to solve the following problem: given a set of memories and sharing rules, identify solutions by defining either a dedicated BIST collar for one memory or a shared BIST collar (parallel or sequential) for a set of compatible memories which minimize the value of the three criteria: area overhead, test power consumption and test time.

Our work led us to formulate a model for the problem, an algorithm for its solution, and a software implementation of both the modelling and the solution steps.

The software is divided into 3 modules, operating in sequence (Figure 1). First, the M_GRP module creates memory compatibility groups. It takes into consideration the collar sharing constraints to build memory sharing groups. The purpose is to make a neat separation between the electronic problem and the mathematical model. This separation is necessary to allow the same software to work for several successive technologies. Then, the M_OPT module finds the best solution by applying genetic algorithms to optimize the memory BIST system. For this optimization, three parameters are considered: area, test time and testing peak power [5, 6]. Finally, M_VAL checks and validates the obtained solutions with respect to sharing constraints, and also serves as a convenient interface to present the solutions to the user.

Numerical evaluation of the proposed solution has been conducted using real-world designs provided by ST Microelectronics. Experiments were performed on designs containing around a hundred memories. A significant reduction is obtained for the three criteria: area, testing peak power and test time compared to the standard approach consisting in having one BIST per memory.
Memories in the design:
Functional clock period, memory parameters, user defined groups…

![Diagram](image)

**Figure 1: Memory BIST Optimizer Software**

**REFERENCES**


