

studPOD : Student Digital Assistant with OS and SIRIUS processor core in FPGA and fully integrated in 0.18µm CMOS

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A new, small, and for low power optimized, Family of Softprocessor cores named SIRIUS-TINY, SIRIUS-JANUS and SIRIUS-HULK has been developed for FPGA as well as for ASIC integration together with a suit of related tools with emphasis on SOC Chips and high performance mixed-signal applications. SIRIUS stands for Small Imprint RISC for Ubiquitous Systems and is developed at the IAF-Offenburg. The core has been verified in several designs from FPGA to full ASIC designs in 0.35 and 0.18 Technologies with high performance, low power and high level language optimized instruction sets. Depending on the application requirement, the selection can be made from this actual Family members.



Performance	SIRIUS-TINY	SIRIUS-JANUS	SIRIUS-HULK
Internal data bus	16 Bit	16/32 Bit	32 Bit
Address space	64kbyte	4GByte	4GByte
OS feasible	BIOS-RTOS	BIOS-RTOS	LINUX
Multiplier	16 x 16	32 x 32	32 x 32
Instruction set	40	58	58
High level Language	C-Compiler	C-Compiler	C-Compiler
Cache-System	No	No	Yes
Verified on ASIC	No	Yes	No
MIPS average / MHz	0.7	0.8	0.9
Logic elements in Cyclone III-FPGA	3000	4200	5400

Clock frequency depending on the technologies 80–150 MHz.

Applications:

- **Electronic pill with remote control (ePille®)**
- **Electrocardiogram recorder/display**
- **RFID semi active sensors**
- **Electro physiological recording and transmission**
- **Implant electronics**
- **studPOD Personal Digital Assistant**
- **Educational designs (FPGA emulator)**
- **VHDL course in the Master degree program (SIRIUS-TINY)**



Fig. 1: PDA with SIRIUS-JANUS (Developed in ASIC Center HS-Offenburg)

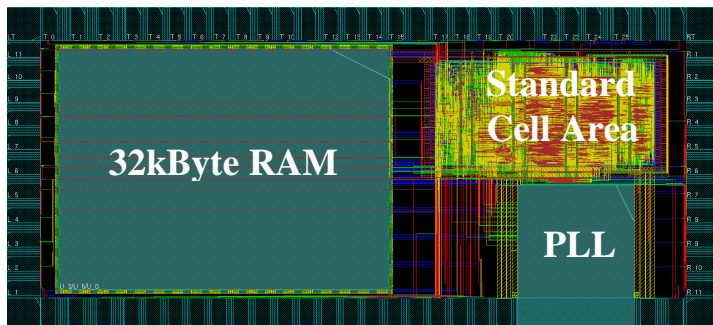


Fig. 2: UMC 0.18µm ASIC SoC (chip area: 3.24x1.53 mm², core only 0.3mm²)

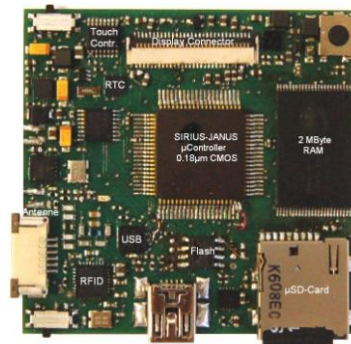


Fig. 3: studPOD board (dimension: 51x53 mm²)

Live demonstration of SIRIUS-JANUS on PDA application and related software development tools