

# Simulator for ZamiaCAD Integrated Hardware Design Environment

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## Abstract

We present a simulator component for ZamiaCAD which is an environment for hardware design entry, analysis, integration and simulation. ZamiaCAD can handle large industrial designs such as the state-of-the-art processors from IBM. It is implemented as a plug-in for the open source Eclipse IDE.

## 1. Introduction to ZamiaCAD

ZamiaCAD (Figure 1) [1] is an integrated hardware design environment for design entry, design analysis, design integration and simulation. In these areas ZamiaCAD targets the automation of currently manual design and verification tasks and hence increases design and verification engineer productivity.

In this demonstration we present a built-in simulator component for this environment (Figure 2).

ZamiaCAD consists of three basic building blocks:

- 1) frontend responsible for HDL parsing,
- 2) the core responsible for intermediate design representation and analysis,
- 3) GUI implemented as a plug-in for Eclipse IDE.

The frontend and the core are about 100K source lines of Java code (SLOC). The Eclipse IDE plug-in is about 20k SLOC.

The frontend is capable of handling full VHDL-93 [2], targets at Verilog (development is at early stage) and has persistent and scalable syntax tree storage. The GUI has graphical viewers and editors and provides for automatic model builder.

The core of ZamiaCAD is based on a powerful, persistent and scalable design database relying on instantiation graph (IG) model. It fully elaborates design model and provides for full source back-annotation and static analysis (e.g. global signal reference search, FSM recognition). The core has interpreter for quick expression evaluation.

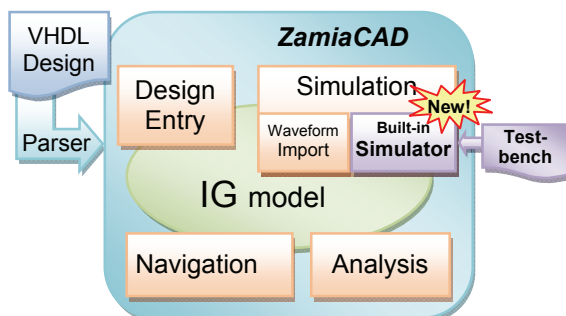


Figure 1. ZamiaCAD structure

## 2. Design Simulation with ZamiaCAD

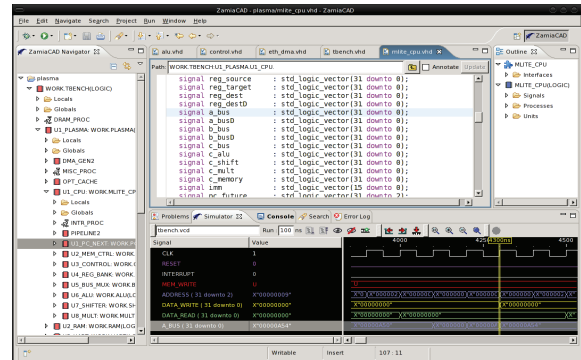


Figure 2. ZamiaCAD with simulator

Design simulation is an important hardware design development task which can be now performed with ZamiaCAD along with other tasks such as design entry, navigation and analysis. The built-in simulator component presented in this demonstration contributes a new feature of ad-hoc design validation in addition to the existing waveform file import modules able to read in Value Change Dump (VCD) files.

The proposed simulator is implemented in accordance with the VHDL standard simulation guidelines [2]. This fact guarantees the correctness of the simulation process, however leaves space for future optimizations. One of the convenient features of the proposed simulator is its support for incremental simulation, which is of a particular use for large design debug.

Currently, ZamiaCAD is under heavy development and has very few early adopters. It is able to handle large industrial processor chips or ASIC chips such LEON3 processor from Gaisler research and state-of-the-art processors from IBM.

## References

- [1] ZamiaCAD webpage: <http://www.zamiacad.com/>
- [2] IEEE Standard VHDL Language Reference Manual, 1993

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