

A High-Level Tool Framework for Exploring and Designing NoC Architectures for 3D ICs

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Abstract—This work presents a framework for high-level exploration and RTL design of an optimized Network-on-Chip (NoC) architecture for 3D chips. The RTL is derived from the high-level exploration methodology in a semi-automated way. FPGA implementation figures are given for various implementation parameters of the Network Interface Element, demonstrating the performance/area trade-off of 3D NoC architectures. Additionally, power consumption measurements for 2D and 3D Network Interface Elements are provided for FPGA prototype implementation.

I. NOC EXPLORATION FOR 3D CHIPS

The 3D NoC exploration methodology is presented in Fig. 1. The starting point of the methodology is an application or a set of applications to be mapped on 3D NoC platform. In order to perform the exploration for alternative topologies of 3D NoC architectures, we have used as a basis the WormSim NoC Simulator [1] that utilizes wormhole switching. This simulator was extended and now supports 3D NoC architectures. Furthermore, the target platforms are three-dimensional heterogeneous NoC platforms employing the vertical interconnection patterns presented in [2]. We define as 3D NoCs these architectures composed of many layers, where each layer is a two-dimensional NoC grid, where the grids are the same for all the layers, composed of elements of the same type. The main objective of the methodology is to derive heterogeneous 3D NoC topologies with a mix of 2D and 3D routers and vertical link interconnection patterns that performs best to the generated traffic based on the application(s) activity.

In order to perform the application mapping, a bandwidth-constrained mapping algorithm was employed [3] and adequately adapted to cover 3D NoC architectures. The mapping decisions are evaluated using a high-level NoC Simulator [2]. The simulation results (average packet latency and energy consumption) reveal which is the 3D NoC architecture that accommodates best the requirements of the application(s).

The proposed 3D NoCs can be constructed by placing a number of identical two-dimensional NoCs on individual layers, providing communication by inter-layer vias among vertically adjacent routers. This means that the position of silicon vias is exactly the same for each layer. Hence, the router configuration is extended to the third dimension, while the structure of the individual logic blocks (IP cores) remains unchanged. The results of this early stage high-level exploration phase are the directives that are passed to next step and used to create the RTL description of the interconnection network.

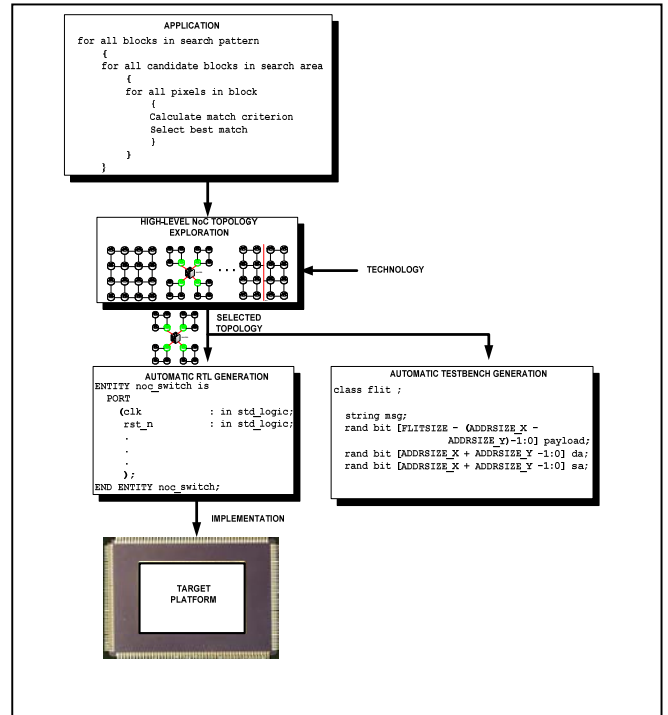


Figure 1. 3D NoC Exploration and Implementation Flow

From the selected topology parameters, selected by the 3D NoC exploration methodology, the RTL description of the selected NoC architecture is derived. The RTL code is based on reusable VHDL network components with parameters selected from a common package file. By generating this file according to the selected topology parameters, the semi-automated VHDL code generation is facilitated. Likewise, the semi-automated generation of testbench files is done in a similar manner.

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