PARO: A Design Tool for Synthesis of Hardware Accelerators for SoCs

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It is a known fact that 90% of the execution time of high performance applications are spent in nested loop programs which offer a tremendous potential of acceleration due to inherent parallelism. Furthermore, streaming applications consisting of multiple communicating loops from fields of signal processing, medical imaging, financial computing require high performance computing. The FPGAs offer huge amounts of resources for realization of massively parallel hardware accelerators. The major goal of the PARO tool developed at the University of Erlangen-Nuremberg is automatic generation of (a) hardware accelerators for FPGAs from algorithms (especially nested loops) descriptions [3], (b) accelerator pipeline, and (c) interface circuits and drivers for system integration. The methodology is based on the intuitive and efficient parallelization in the polytope model [2]. There exists only a few tools for hardware generation like PICO from Synfors that are also based on the polytope model. The design trajectory of PARO is shown in Fig. 1. The novelty of the tool design flow is summarized as follows:

- For design entry, a new language for dataflow-based algorithm description as communicating nested loops is used. The language can be used both for behavioral description as well as architecture description.
- New multilevel partitioning technologies for balancing memory hierarchies and communication requirements. Several other advanced transformations like localization and standard compiler optimizations like common subexpression elimination, and others [5] are also available in the high level transformation toolbox for obtaining amenable algorithm description in terms of data reuse and resource usage.
- Scheduling based on Mixed Integer Linear Programming (MILP) with modeling of resource constraints, speculative execution, software and functional pipelining [4].
- Functional simulation and Modelsim simulation at different levels of design flow for validation.
- Automated synthesis of communication subsystem for communication between accelerators in a pipeline based on a novel dataflow model of computation.
- Automated generation of memory map, interface circuits and device driver for integration of accelerators in SoC architectures.
- Design space exploration
- The PARO backend produces an intermediate RTL representation which is retargeted to VHDL.

Advantages of the tool as compared to other tools lies in

- Compact and intuitive representation (big operators like

\[ \sum_k \mathbb{P}_k \] of input algorithm in the language.
- Optimal hardware generation in terms of performance, leveraging the available parallelism in the algorithm with respect to resource constraints.
- Automatic generation of an Input/Output interface for the hardware accelerator for integration in System-on-Chip on an FPGA.

State-of-the-art medical imaging applications from industry have been successfully synthesized with PARO tool [1].

REFERENCES