A Practical Scan Optimization Algorithm at the Register Transfer Level

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Abstract

Scan insertion at the RTL level holds great promises. While previous attempts at RTL-scan have not been convincing, a novel mathematical approach for one-pass scan chain stitching at RTL is proposed.

1. Introduction

These days, the cost of manufacturing chips approaches the cost of testing them. So the semiconductors community needs low cost and high quality test solutions. New and efficient DFT solutions are greeted with higher expectations than ever. Current DFT solutions result in unpredictable design development time and development costs and directly impact time to market.

Because scan allows better control and observation of internal design logic, it is widely adopted for manufacturing testing and other purposes. However, traditional scan solutions make such an extension very difficult since engineers need to handle gate-level netlist without benefiting from what happens during synthesis. Also, scan implementation decisions are considered post-synthesis. This is too late in comparison to RTL design decisions. Adopting scan at the RTL level will cover new design and manufacturing needs, strengthen verification and consolidate reusable design methodologies by closing the gap between RTL and design for test. There are many advantages to inserting scan at the RTL level like benefiting from the synthesis process (i.e. better optimisation in terms of area and timing).

It is now possible, using EDA tools such as HiDFT-Scan from DeFacTo Technologies, to consider scan at RTL.

Within this framework, the objective of this work is to demonstrate the feasibility of implementing scan at RTL. Indeed, the proposed algorithms lower the impact of RTL scan chain insertion before synthesis. This is measured through deep analysis at the physical level (i.e. layout) and is compared to existing post-synthesis scan implementation results.

Scan chain insertion at the RTL level has been investigated in [1] and more recently in [3]. This work complements [1] in that no stitching ordering was proposed there.

2. Experimental flows

The traditional scan insertion flow is illustrated in Fig 1. In such a flow, scan chains are inserted after the logic synthesis process. For gate level scan several iterations around placement and routing are required to find a good stitching order.

In Fig. 2, scan is inserted at the RTL level, before synthesis. The aim is to build and sign-off optimal scan chain architecture in one pass at the RTL level instead of several iterations at the gate level. Indeed, after the introduction of the scan chain at the RTL level scan memory elements are mixed with the others elements of the design, no restitching is required. The algorithm which is proposed for RTL scan stitching decisions is described in the next section.

3. Methodology

The difficulty with one pass scan chain stitching is to find an ordering of the memory elements that minimizes the impact of test circuitry on chip performance (area overhead, function and test power, etc.) and on the cost of the design with no layout information at our disposal. This research work helps in solving stitching decisions at RTL when scan chains are built. For this we propose an algorithm that finds a scan chain stitching which minimizes the global wire length. In fact, this parameter has a large impact on
routability, and power consumption of the design. The RTL description of the design is translated into a graph. The extracted graph represents information from the RTL description like the proximity of the memory elements of a scan chain: connected flip-flops, geometric proximity on the final physical design etc. Using this graph, research of scan chain ordering is reduced to a travelling salesman problem (TSP), which is a classical problem in combinatorial optimization. This problem is often used for scan restitching using some data extracted from layout like in [5]. To solve this NP-complete problem we use an efficient algorithm which is a 2-approximation. It is a well known heuristic (in literature) [2, 4]. The running time of this algorithm is $O(n+m \log n)$, where $n$ is the number of flip flops and $m$ the number of edges of our graph.

5. Numerical results

The goal of the experiments we performed is to measure the total wire length of a chip obtained after placement and routing from the proposed scan chain ordering at the RTL level. We also compare these results with the scan before synthesis at the gate level. Experimental results on test cases in Verilog and VHDL are summarized in the table below:

<table>
<thead>
<tr>
<th>Circuit</th>
<th># Flip flop</th>
<th>RTL</th>
<th>Wire length (gate)</th>
<th>Wire length (RTL)</th>
</tr>
</thead>
<tbody>
<tr>
<td>b03</td>
<td>30</td>
<td>vhdl</td>
<td>1,790</td>
<td>1,772</td>
</tr>
<tr>
<td>b04</td>
<td>66</td>
<td>vhdl</td>
<td>6,303</td>
<td>6,498</td>
</tr>
<tr>
<td>b13</td>
<td>53</td>
<td>vhdl</td>
<td>3,394</td>
<td>3,318</td>
</tr>
<tr>
<td>b15</td>
<td>449</td>
<td>vhdl</td>
<td>126,316</td>
<td>121,829</td>
</tr>
<tr>
<td>simple_spi</td>
<td>132</td>
<td>verilog</td>
<td>11,459</td>
<td>10,433</td>
</tr>
<tr>
<td>Biquad</td>
<td>204</td>
<td>verilog</td>
<td>34,103</td>
<td>31,328</td>
</tr>
</tbody>
</table>

For each test case, total wire length including original interconnections is presented. Columns 2 and 3 give the RTL description language (VHDL or Verilog) and the number of flip flops in the circuit. Next, we present the total wire length after scan insertion in the gate level and in the RTL level. Scan at the gate level is inserted by Magma’s integrated flow; scan at the RTL level is inserted with HiDFT-Scan from DeFacTo technologies. These results show that the proposed method reduce the total wire length as compared to the gate level. Finally, scan at the RTL level does not degrade the total wire length of the layout.

6. Conclusion

In this work, we propose a new approach to insert scan chains at the RTL level. Our aim is to limit the impact of scan in the design by minimizing the total wire length of the scan chain. The solution is based on a mathematical model from graph theory. The scan chain stitching at the RTL level is modelled as a travelling salesman problem (TSP). Experimental results presented show that the method can be used on real designs both in Verilog and VHDL. The proposed method reduces the total wire length and improves both the design performance and testability.

7. References


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