

## TUTORIALS

### **A Automatically Realising Embedded Systems from High-Level Functional Models**

Organiser: Pieter J Mosterman, The MathWorks, US  
Speakers: Don Orofino, The MathWorks, US  
Janos Sztipanovits, Vanderbilt U, US  
Ahmed Jerraya, CEA-LETI, FR  
Wido Kruijtzter and V Reyes, NXP, NL  
Christos Cassandras, Boston U, US  
Grant Martin, Tensilica, US

To keep pace with the rising computational demands of embedded applications, an effective approach is to raise the level of abstraction at which the design of essential functionality is performed. Raising the level of abstraction allows designers to remove the complexity of low-level and implementation details, thereby gaining design productivity. However, raising the level of abstraction also widens the gap between design and implementation. To overcome the gap between design and implementation, this tutorial demonstrates technologies for

- (i) the automatic transformation of the design into increasingly detailed representations,
- (ii) checking correctness of the additional detail, and
- (iii) hardware/software codesign.

Model-Based Design is introduced and experts from industry and academia demonstrate the use of technologies such as automatic C and HDL code generation, automatic test bench generation, automatic sequential design refinement, and multi-domain system design, including mixed-signal simulation. The attendees will learn how to develop high-level domain specific models of embedded systems and how to exploit automatic transformation technology to systematically realise the embedded application.

### **B Design Flows, Communication Based Design and Architectures in Automotive Electronic Systems**

Organisers: Juergen Becker and Michael Huebner, Karlsruhe U, DE  
Speakers: Juergen Becker, Karlsruhe U, DE  
Michael Huebner, Karlsruhe U, DE  
Robert Esser, Xilinx, Dublin, IE  
Andreas Herkersdorf, TU Munich, DE  
Walter Stechele, TU Munich, DE  
Vera Lauer, DaimlerChrysler AG, DE

A steadily increasing number of microprocessors and electronic components with the heavy demand of computation performance in automotive electronic systems affect substantially the design of networked ECUs in today as well as future cars. Novel approaches, based on heterogeneous hardware (Coarse- fine Grained reconfigurable Hardware, Microprocessors) could be a solution to handle the computation intensive tasks, e.g. for driver-assistance systems. The challenge here is to find an optimal trade-off between power consumption, cost, performance and flexibility which leads to the question which technology and which distribution (automotive function centralisation - decentralisation trade-offs!) will be targeted in future car electronics. Introducing novel architecture topologies and corresponding tool flows with standardised specification and verification are here severe challenges. A first approach to meet these challenges is the AUTOSAR development partnership, which aims at a standardisation of automotive software architecture.

The purpose of this tutorial is to evaluate and discuss new concepts for communication based design of automotive electronic and car network systems, as well as to discuss and envisage future system design in automotive electronics. Both aspects, hardware / software design and tool-integration will be discussed. The main emphasis in this session is design-flow, tool-development, applications and system design. The tutorial is addressed to hardware and system engineers as well as to researchers. A set of presentations intended to set the stage for the discussion, will be followed by a panel where selected world-wide specialists in the field of automotive electronics will discuss the demands and interests of industry on novel technologies and systems and research activities for future automotive systems.

### **C System-Level Design and Application Mapping for Wireless and Multimedia MPSoC Architectures**

Organiser: Rainer Leupers, RWTH Aachen, DE  
Speakers: Rainer Leupers, RWTH Aachen, DE  
Gerd Ascheid, RWTH Aachen, DE  
Wilfried Verachtert, IMEC, BE  
Tom Ashby, IMEC, BE  
Arnout Vandecappelle, IMEC, BE

Advanced embedded devices such as multi-standard mobile terminals demand ever-increasing performance and energy efficiency. Simultaneously, a high degree of flexibility and programmability is required due to increasing software complexity and fast changing protocol and codec standards. This has led to the concept of MPSoC (Multi-Processor System-on-Chip) platforms. In many cases, MPSoCs are simply assembled in "best effort" manner from existing legacy IP components, and programming the platform presents a major bottleneck. As Moore's Law permits us to enter the "many core" MPSoC area, what is needed is a systematic approach that builds on well-proven technologies, but also innovates with novel classes of electronic system-level (ESL) design automation tools.

This tutorial discusses several key questions with significant impact on the future of MPSoC: What are the MPSoC killer applications? Is homogeneous or heterogeneous architecture the right choice? What are the key tools, methodologies and programming models for successfully designing and programming MPSoC platforms? In the end, will there be only a few survivor platforms that everyone has to accept? Based on their extensive research and industry experience, the presenters will provide their answers from a practical, application-oriented perspective.

#### **D1 Design Variability: Challenges and Solutions at Microarchitecture-Architecture Level**

Organiser: Diana Marculescu, Carnegie Mellon University, US  
Speakers: Diana Marculescu, Carnegie Mellon University, US  
Sani Nassif, IBM, US

Driven by aggressive technology scaling and sub-wavelength lithography, there has been a marked increase in the variability of process technology parameters. In addition, due to increased power density and stricter thermal envelopes, environmental parameter variability (e.g., temperature and voltage variation) increases as well. While a significant body of work exists for characterising performance and power consumption in the presence of process-driven variability at the interface between physical-gate levels, these effects need to be modelled at higher levels of abstraction as well. Current high-level design methodologies targeting architecture and system levels still assume a classic static timing behaviour and do not include effects of variability on performance or energy. In support of a complete probabilistic design flow, high-level modelling of variability effects is needed for determining design choices that are most likely to meet initial design constraints. This objective becomes even more important in the case of complex multi-core designs that are unable to be analysed by existing variability-aware tools.

The tutorial will cover the basics of design variability and how this information can be used at microarchitecture/architecture/system levels for correctly assessing performance and power consumption and their likelihood of satisfying given constraints.

#### **E1 Power Gating for Ultra-low Leakage: Physics, Design, and Analysis**

Organiser: Jerry Frenkil, Sequence Design, US  
Speakers: Jerry Frenkil, Sequence Design, US  
Ken Choi, Illinois Institute of Technology, US  
Kimiyoishi Usami, Shibaura Institute of Technology, JP

The demand for portable electronic devices continues to grow rapidly and has generated great interest in low power design, which initially focused on controlling dynamic power consumption. However, the combination of wireless device operational characteristics and exponentially increasing leakage power in new processes motivated the development of leakage reduction techniques.

Power gating has emerged as the most effective design technique for achieving ultra-low leakage power. While conceptually simple, in practice power gating is difficult to implement efficiently. This tutorial will provide detailed descriptions of the physics, motivations, benefits, challenges, techniques, methods, and tradeoffs associated with the design of power gated circuits.

Intended for designers and managers of low leakage SoCs and related design automation, this tutorial will provide a detailed view of power gating. Attendees will learn not only how to develop power gated circuits, but also why to use power gating, when to choose it over or in conjunction with other leakage control techniques, and the issues power gating presents on different aspects of design flows.

#### **F1 Heterogeneous System-level Specification Using SystemC**

Organiser: Eugenio Villar, Cantabria U, ES  
Speakers: Eugenio Villar, Cantabria U, ES  
Axel Jantsch, KTH, SE  
Christoph Grimm, TU Vienna, AT  
Tim Kogel, CoWare, DE

Every development of a complex, heterogeneous embedded system today is model based. Sound and well understood models are a necessary basis for all design, analysis and verification activities. However, most modelling practices used by industry often lack of methodological foundations being based on 'ad-hoc' solutions. But as it will be shown in this tutorial, theoretical concepts of Models of

Computation and Communication (MoCC) can still be of practical use in industrial design flows by use of proper libraries, methodologies and modelling rules.

In this tutorial we will present and discuss theoretical foundations of MoCCs, as they have been developed during the last 15 years. We will show how these concepts facilitate the clean, deterministic integration of heterogeneous modelling domains, such as analogue, continuous time models, discrete event models, dataflow models and models of concurrent programming.

We will then demonstrate how the theoretical insight can be packaged into a methodology; modelling rules and design libraries for use in a SystemC based industrial design flow above the current TLM standard.

The tutorial will present ForSyDe as the theoretical framework for system specification. Then, HetSC, a SystemC specification methodology and associated library for heterogeneous, system specification and design will be described. SystemC AMS will be proposed for mixed analogue-digital modelling. Finally, the tutorial will address system modeling using TLM. The last version of the standard, TLM2 will be introduced.

## **G1 Power-Aware Testing and Test Strategies for Low Power Devices**

Organisers: Dimitris Gizopoulos, Piraeus U, GR and Kaushik Roy, Purdue University, USA

Speakers: Patrick Girard, LIRMM, FR  
Nicola Nicolici, McMaster University, CA  
Xiaoqing Wen, Kyushu Institute of Technology, JP

Power dissipation is becoming a critical parameter during manufacturing test as the device can consume much more power during test than during functional mode of operation. In the meantime, elaborate power management strategies, like dynamic voltage scaling, clock gating or power down techniques, are used today to control the power dissipation during functional operation. The usage of these strategies has various implications on manufacturing test, and power-aware test is therefore increasingly becoming a major consideration during design-for-test and test preparation for low power devices. This tutorial provides knowledge in this area. It is organised into three main parts. The first one gives necessary background and discusses issues arising from excessive power dissipation during test application. The second part provides comprehensive knowledge of structural and algorithmic solutions that can be used to alleviate such problems. The last part surveys low power design techniques and shows how these low power devices can be tested safely without affecting yield and reliability.

The tutorial is targeted towards Test and Design-for-Test practitioners (engineers, engineering managers, students, academics) who are interested in learning more about the impact of power dissipation during manufacturing test, how it is possible to alleviate test power issues, and how low power devices can be tested safely without affecting yield and reliability.

**This tutorial is part of the IEEE Computer Society TTTC Test Technology Educational Program (TTEP) 2008**

## **D2 From Transistor to PLL – Analogue Design and EDA Methods**

Organiser: David M Binkley, U of NC at Charlotte, US

Speakers: David M Binkley, U of NC at Charlotte, US  
Helmut Graeb, TU Munich, DE  
Georges G E Gielen, KU Leuven, BE  
Jaijeet Roychowdhury, U of Minn Twin Cities, US

Although analogue and mixed-signal design is greatly complicated by numerous design choices, the management of these design choices presents significant opportunities for optimising designs for desired tradeoffs in performance and high production yield. This tutorial describes analog design and EDA methods beginning with MOS transistors and concluding with PLLs as complete mixed-signal systems.

Tutorial topics include: (1) tradeoffs and optimisation in analogue CMOS design through transistor drain current, inversion coefficient, and channel length selections; (2) transistor sizing rules, rules for transistor groups, and robust Pareto optimisation of circuits; (3) analogue synthesis, hierarchical design, and yield optimisation; and (4) behavioral modelling of oscillators and PLLs using nonlinear phase macro models that capture jitter and phase noise, injection locking, PLL lock and capture phenomena, and cycle slipping. Tutorial topics are interrelated with each other and illustrated using actual designs. Finally, future directions for analogue design and EDA are suggested, including applications to biological systems such as mammalian circadian rhythms.

This tutorial is targeted to analogue and mixed-signal designers, EDA developers and users, design managers, and advanced university students.

## **E2 DfM in the Analogue and Digital World**

Organisers: Carsten Elgert, Mentor Graphics, DE  
Speakers: Volker Herbig, X-Fab, DE  
Anton Ossner, Chartered Semiconductor, DE  
Thomas Harms, IFX, DE  
Emmanuel Blanc, Mentor Graphics, FR

No matter whether the designer thinks analogue or digital, he is faced with the DfM issue. Although confronted with different challenges, the key for satisfying yield in production lies in the design phase. Tools, techniques, and methods that once worked without fail cannot hold up any longer. More of the responsibility for yield must shift to the designer, so the fabless model, where foundry information flows freely, increases in importance.

As we dive deeper into the nanometer space, we must even completely rethink the way we design at the 65 and 45 nm depths, making it more challenging than ever to achieve yield. Not only are more DRC rules required, but the rules are becoming much more complex in light of more manufacturing issues. Yet advanced DRC is still not enough. We must redefine the sign-off process itself to include a spectrum of new methods that assess design quality.

In the nanometer age, sign-off must include not only fundamental, rule-based physical verification and parasitic extraction, but also a set of automated technologies that help improve yield by enhancing the design itself. DFM solutions must deliver these automated technologies to the designer in a practical and easy to use way. We need new ways to visualize and prioritize the data produced by the analytical tools. Existing tools need expanded architectures to provide yield characterisation and enhancement capabilities. The most successful DFM methodologies in the nanometer age will apply these new capabilities throughout the design flow — not just at the point of sign-off.

This tutorial goes into detail on these new technical challenges and solutions within both the business and historical context of the IC design and manufacturing process. It shows the importance of the fabless model as part of a more holistic DFM methodology.

## **F2 Formal Methods in System and MpSoC Performance Analysis and Optimisation**

Organiser: Rolf Ernst, TU Braunschweig, DE  
Speakers: Rolf Ernst, TU Braunschweig, DE  
Marek Jersak, Syntavision, DE  
Hans Sarnowski, BMW, DE  
Marco Bekooij, NXP, NE  
Samarjit Chakraborty, National U of Singapore, SG

Formal analysis and optimisation of networked real-time systems has reached industrial maturity and is now regularly used, e.g. in automotive system design. More recently, such formal methods have been extended to MpSoCs, as a complement to simulation in order to improve predictability and reach performance guarantees.

The tutorial starts with an introduction to formal platform performance analysis covering the main communication and resource modelling techniques and their application to embedded systems and MpSoC. Next is an overview on industrial applications and experiences followed by a comprehensive use case from automotive design which demonstrates how to acquire the necessary model data. The fourth presentation provides an approach to predictable MpSoC platform sharing using service shaping concepts and a corresponding formal performance analysis approach. The current performance models largely abstract from component state information to reach manageable computation times, at the cost of some loss of modelling precision. The tutorial closes with an overview on how to combine state-based and functional models for MpSoC in a single analysis to improve modelling precision.

## **G2 Soft Errors: System Effects, Protection Techniques and Case Studies**

Organisers: Dimitris Gizopoulos, Piraeus U, GR and Kaushik Roy, Purdue U, US  
Speakers: Subhasish Mitra, Stanford U, US  
Pia Sanda, IBM, US

Radiation-induced soft errors are getting worse in digital systems manufactured in advanced technologies. Stringent data integrity and availability requirements of enterprise computing and networking applications demand special attention to soft errors in sequential elements and combinational logic. This tutorial will discuss the impact of technology scaling on soft error rates, system effects of soft errors, actual data on system behaviours in the presence of soft errors from latest systems, CAD techniques for quantifying soft error vulnerabilities, design of architectures with Built-in-Soft-Error-Resilience techniques, and actual case studies of protection techniques.

**This tutorial is part of the IEEE Computer Society TTTC Test Technology Educational Program (TTEP) 2008**