

PWM-Based Test Stimuli Generation for BIST of High Resolution $\Sigma\Delta$ ADCs

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A fully digital test stimuli generation and on-chip specifications evaluation for cheap, fast, though accurate testing of high resolution $\Sigma\Delta$ ADCs are here presented. Simulations and measurements showed a discrimination threshold on specification parameters up to -90 dBc. The proposed method helps reduce the cost of ADC production test, to extend test coverage and to enable Built-In Self-Test and test-based self-calibration.

1. Introduction

Most of today's ADCs are deeply embedded, which adds significant extra difficulties in testing. Built-In Self-Test (BIST) is the most promising solution to test those deeply embedded ADCs. Numerous efforts have been spent on trying to integrate high accuracy stimulus sources on-chip to accomplish ADC BIST [1-7]. However, the on-chip implementation of sufficiently high accuracy stimulus sources is extremely difficult. Reported on-chip stimulus sources either require too much design effort and die area, or lack the capability to test ADCs with high resolution. In fact, for testing ADCs with 16-bit or higher resolutions using the conventional histogram method or the FFT, more than 20-bit linear signals are needed and more than 13,000 samples have to be processed to reach -90 dB of discrimination threshold on each specification evaluation. This paper describes a new method to generate a fully digital test signal allowing the simultaneous evaluation of the most important specifications for audio $\Sigma\Delta$ ADCs saving test time. In [7] the presented technique used RTL-Synthesized logic on-chip and trivial off-chip analog components, i.e. low pass RC filters to generate four exponential steps using a digital pulse-width modulated waveform. This analog circuit however, though simple cannot be accommodate on-chip. The method described here uses a test stimulus which is purely digital. Thus, the test signal generation can be easily implemented on-chip. In a previous work [8, 9], the authors presented results for an ADC test algorithm based on a Pulse Width Modulated (PWM) test signal generated by an FPGA. Here simulations and experimental results are reported, showing a discrimination threshold of -80 dBc on the 2nd harmonic distortion (HD) and -90 dBc on the 3rd HD, THD, SINAD and SNR evaluation. The test signal generation simplicity makes the proposed technique promising for BIST implementation. The proposed technique has been patented [9].

2 PWM signal as test stimulus

It is well known that the $\Sigma\Delta$ ADC [9] processes the integral of the input signal (output of the modulator block) and is partially insensitive to the detailed shape of the input signal within each sample clock period.

As a consequence of that, any randomly shaped signal behaves nearly as if it was constant over the whole sample clock period and equal to the average value (i.e. the integral) over the clock period itself.

The $\Sigma\Delta$ ADC sensitivity to the integral (if analog) or to the sum (if switched capacitor) of the input samples, more than to the input signal shape itself, has been used in this work to determine a low cost test stimulus that can be easily generated and allows an accurate prediction of the analog specifications. The synchronous PWM is a good candidate to achieve the desired goal. A synchronous PWM signal is a purely binary waveform (therefore easy to be generated), whose frequency coincides with the sample rate F_S . In the following it will be indicated with T_L and T_H the PWM signal's low and high pulse width, respectively. The high and low values are two reference levels V_{refL} and V_{refH} , respectively, that could be generated internally, without requiring additional external circuitry (e.g. in a CODEC, the references of the DAC). By using a PWM signal at the input of the ADC, the equivalent input signal is:

$$V_{eq} = V_{refL} T_L + V_{refH} T_H = V_{refL} + (V_{refH} - V_{refL}) \eta \quad (1)$$

where $\eta = T_H / (T_L + T_H)$ is the PWM duty-cycle.

In particular, a PWM signal synchronous with the sample period and with a duty-cycle $\eta(t_i)$ which varies at each i -th sample, is seen by a $\Sigma\Delta$ ADC as an equivalent analog voltage:

$$V_{eq}(t_i) \approx V_{refL} + (V_{refH} - V_{refL}) \eta(t_i) \quad (2)$$

where $V_{eq}(t_i)$ is the *equivalent input voltage* seen by the ADC.

Following the proposed approach, it is sufficient to generate an appropriate PWM waveform with a suitable duty-cycle, to emulate the desired analog test signal $V_{eq}(t_i)$ and to process the ADC output to estimate the ADC performances. The next sections describe some detailed solutions.

2.1 Dynamic Range of the Input Stage

A time-continuous signal stimulates the input stage correctly if slowly swinging inside the ADC dynamic range (i.e. a ramp or a sinewave). The purely digital PWM signal, fast switching between the high and low value can cause the ADC saturating or, more likely, forces it to work in the non-linear region determining a so-called “slope-overload condition”.

In reality the signal transfer function of the modulator represents the input signal by the output sequences, delayed by one sampling clock period. The transfer function does not contain any bandwidth limitations of the input signal. Any input signal within the range can be processed by the sigma-delta modulator, including e.g., discontinuous signals with step-like transitions. For the modulator, if the signal at the input is within its input range $[-a, +a]$, the magnitude of the maximum slope of the accumulated sequence is anyway a/T (with T the sampling period), whatever kind of signal is at the input. Thus, the delta modulator can always track its input, and the slope-overload condition cannot occur. To compare how the two signals a sine-wave and the PWM are seen from the modulator stages, a fourth-order discrete-time $\Sigma\Delta$ ADC, shown in fig. 1 (where the proprietary coefficient values have been masked out), have been simulated. The signals at the output of each stage have been compared. Figure 2 shows the signals at the output

of each modulator stage, while fig. 3 shows the signal at the output of the decimator filter (not shown in fig. 1).

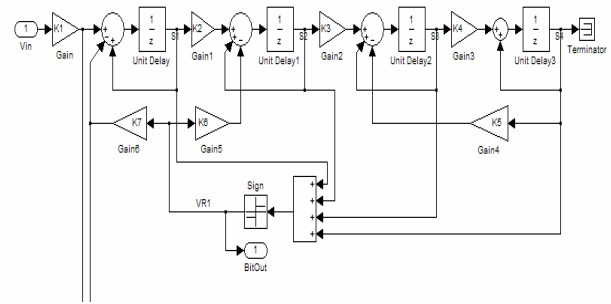


Figure 1 Block diagram of a fourth order single loop $\Sigma\Delta$.

The figures 2 and 3 show the simulation results achieved for a pure $2 V_{pp}$ sine-wave (left side) input stimulus and for a PWM signal with a sinusoidal duty-cycle variation (right side) one. It can be seen that in both cases the waveforms are similar, except for a higher level of noise when the PWM signal is applied. Also the RMS value at the input of the first switched capacitor integrator (the differential input stage) has been monitored under the two different conditions. The results are $0.265V_{RMS}$ and $0.280V_{RMS}$, respectively when the sine-wave or PWM signal are applied, which proves the consistency of using the PWM signal instead of the traditional sine-wave.

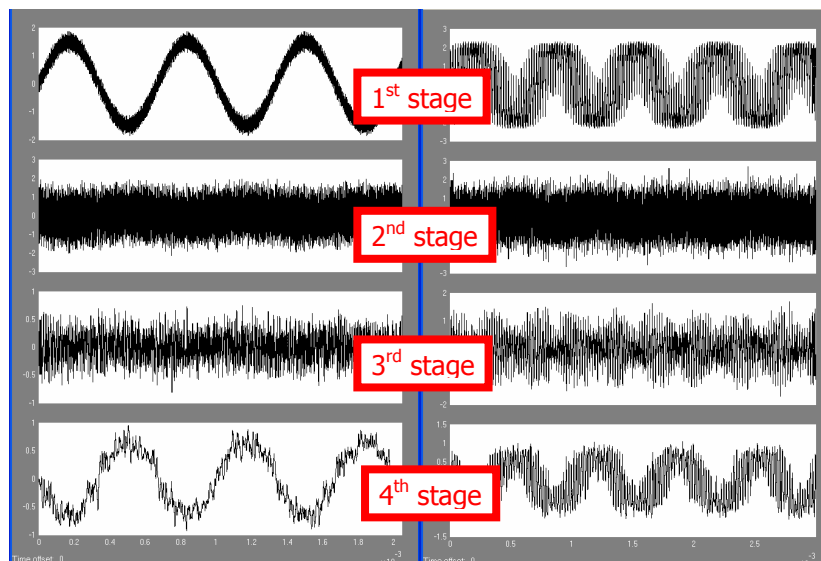


Figure 2 Outputs of the four stages of the $\Sigma\Delta$ modulator depicted in fig. 1, when at the input of the modulator is a pure analog sinewave (left plot) and when instead a PWM signal with a duty-cycle varying sinusoidally, at the same frequency (right plot) is used.

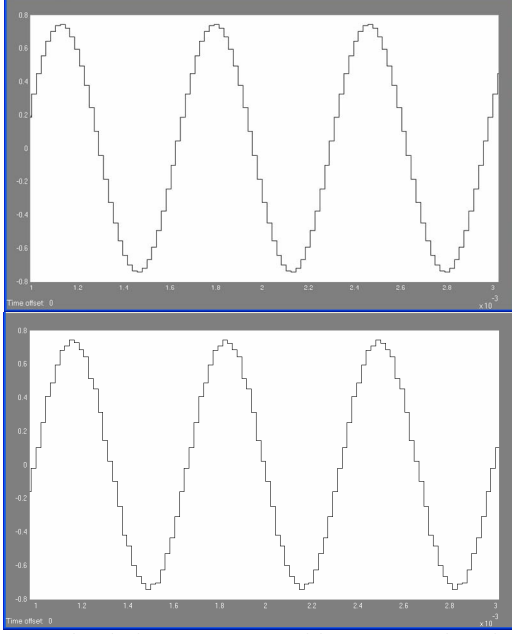


Figure 3 The decimator outputs with a pure analog sine wave (on the top) and with a PWM signal with a duty-cycle varying sinusoidally with time, at the same frequency (bottom plot).

2.2 Effects of High Frequency Components

Another aspect to be investigated to validate the test signal is to study the impact of the high frequency spectral components generated by a PWM signal. A pure sine wave has no spectral component above the Nyquist frequency, while a PWM signal has spectral components above that value. It is therefore important to assess what are the effects of those components on the ADC output.

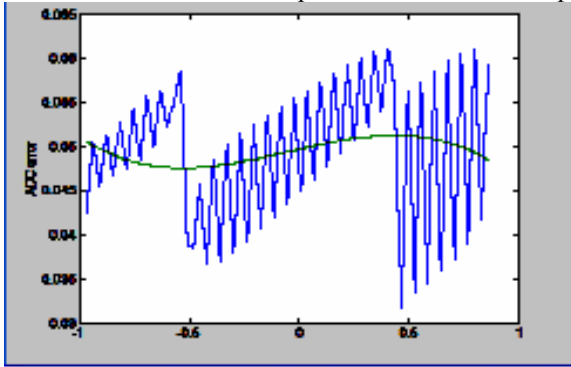


Figure 4 The difference between decimator outputs in presence of a sine wave at the ADC input and when a PWM signal is applied, versus the equivalent input voltage, and its third-order polynomial fitting.

This aspect has been addressed by detailed simulations on the $\Sigma\Delta$ modulator (fig. 1) and its decimator filter. Figure 4 depicts the difference between the two output signals when a sine-wave and PWM are applied, respectively. The difference, in the order of -70dBc, is due to the PWM signal and shows the small error affecting formula (1). Figure 4 also shows the 3rd order

polynomial fitting. Since this artefact is predictable (from simulation), the measurements can be compensated by properly post-processing test results.

3. The PWM test signal

The proposed technique is based on the generation of a binary waveform with a period equal to the ADC sampling period $T=1/F_S$ and a variable duty-cycle as test stimulus. The duty-cycle $\eta(t_i)$ varies at every i -th sample period, while the voltage levels are calibrated, by means of a simple 1-bit DAC. For each i -th sample, the value of the equivalent analog value $V_{eq}(t_i)$ is given by:

$$V_{eq}(t_i) = V_{refL} + (V_{refH} - V_{refL}) * (\eta(t_i) - \alpha) \quad (3)$$

where α is a constant correction factor, taking into account the constant rise and fall times of the binary signal and the 1-bit DAC. The converter detects the equivalent voltage $V_{eq}(t_i)$ and converts it into an n -bit digital value:

$$Y(t_i + \delta) = 2^n (\eta(t_i) - \alpha + \varepsilon'(\eta(t_i))) \quad (4)$$

where δ is the ADC latency, mostly due to the decimator. The ADC introduces an error $\varepsilon'(\eta) = \varepsilon(V_{eq})$ due to its non ideal properties: non-linearity, quantization noise, harmonic distortion, thermal noise etc., which are the converter specifications to be evaluated during the test. Therefore gain, 2nd and 3rd Harmonic Distortion (HD) can be evaluated by knowing $\varepsilon'(\eta)$, while the offset cannot be determined exactly, since the factor α is usually unknown. By varying the duty-cycle $\eta(t_i)$ in a suitable way, the ADC error is, using (4):

$$\varepsilon(t_i) = \frac{Y(t_i + \delta)}{2^n} - \eta(t_i) + \alpha \quad (5)$$

The proposed technique can be practically implemented at least in two different ways [9]: by using a *linear PWM* or a *sine-wave PWM*, as described in next sections.

3.1 The Linear PWM Test

The *linear PWM approach* consists of generating a test PWM waveform, with a duty-cycle linearly increasing with time: $\eta(t_i) = \frac{i}{N}$, $0 < i < N$ with, e.g. $N=64$. The number

N of steps affects the accuracy on the ADC specifications. The ADC will sample and convert the linear input sequence and generate the digital sequence given by (4). The $N-1$ polynomial fitting expresses $\varepsilon'(\eta)$ as a 3rd order polynomial:

$$\varepsilon'(\eta) \approx \varepsilon_0 + \varepsilon_1\eta + \varepsilon_2\eta^2 + \varepsilon_3\eta^3 + \gamma \quad (6)$$

where $\varepsilon_0, \varepsilon_1, \varepsilon_2, \varepsilon_3$ are the polynomial coefficients, while γ is the null-average ADC noise. By analyzing the $N-1$ output samples $\frac{Y(t_i + \delta)}{2^n} - \eta(t_i)$ with a 3rd order

polynomial regression technique, it is possible to evaluate

the 3rd order (or even higher) polynomial, which better fits the ADC characteristics.

3. 2 The Sine-Wave PWM Test

As she *linear PWM approach* measures ADC specifications in the time domain, the *sine-wave PWM approach* does the same in the frequency domain. It generates a digital test stimulus characterized by a duty-cycle variable as a sinusoidal sequence:

$$\eta(t_i) = \text{round} \left(\frac{1 + \sin\left(\frac{2\pi i}{N}\right)}{2} \right) \quad (7)$$

where N is again the number of samples (e.g. N=64). If the input sequence (7) is perfectly sinusoidal, the FFT of the output sequence $Y(t_i)$ would give the offset and gain errors together with 2nd, 3rd and higher order HD and SNR. Since the discretization of input signal is perfectly deterministic, the undesired harmonics at the input can be computed theoretically and subtracted.

4. Experimental results

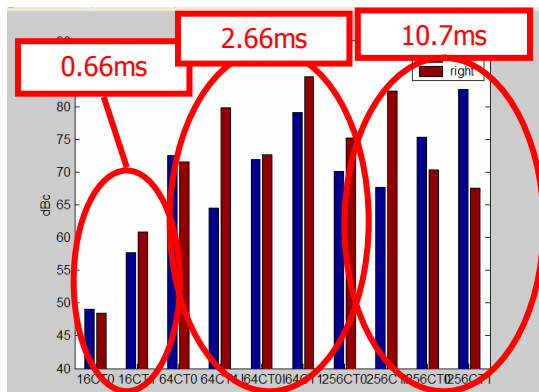


Figure 5: Measured 3rd HD for different test time.

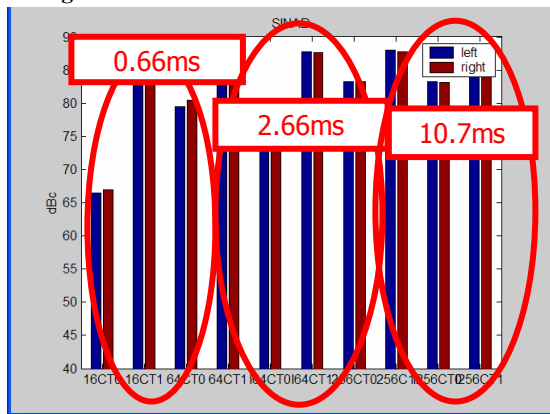


Figure 6: Measured SNR for different test time.

The proposed approach has been validated on a commercial device (a Burr-Brown PCM3002, 20-bit codec). A preliminary simulation of the system has been performed by using CodeSimulink [10], a tool that allows

the calibration of the test procedure and to program the FPGA. Experimental results have been obtained by means of a test board. The stimuli generation and post-processing have been performed by the Altera Flex10K50 FPGA. The board allows to feed a clean sine-wave at the input of the ADC, to compare test results achieved with the traditional FFT test for different test times: 0.66ms (N=16); 2.66ms (N=64); 10.7ms (N=256). The 2nd HD, the 3rd HD and SNR have been evaluated and some results are shown in fig. 5 and 6. On the x axis the number of samples (16, 64, 256), the channel and the considered starting sample of each ramp are indicated. The best compromise has been achieved with 2.66ms test time, triangular waveform. The measured 2nd HD is 74dBc \pm 1.5dB and 3rd HD is -80dBc \pm 2dB (fig. 5). The left channel shows a different behaviour due to deviation between the two channels. Figure 6 shows the SNR measured with the proposed method.

5. Conclusions

This paper described a novel approach for the test of $\Sigma\Delta$ ADCs, which can be used both for production test and for calibration. The proposed method is able to evaluate the converter gain, offset, 2nd and 3rd HD and SNR, at the same time during the test. Measurements on a commercial $\Sigma\Delta$ ADC (PCM3002 CODEC) demonstrate a threshold discrimination capability of -74 dBc on the 2nd and -80dBc on the 3rd HD and -90dBc on SNR in 2.66ms test time. The few gates needed for the method implementation make it suitable for BIST purpose.

6. References

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