

# Implications of Technology Trends on System Dependability

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CMOS has been the dominant integrated circuit (IC) technology for nearly four decades, following the trends predicted by Moore's Law, and fueling the information and communication revolution. As chip geometries decrease and transistor densities increase, new types of faults – from manufacturing defects and operational transients to long-term wearout – need to be addressed. These faults and the resulting logic errors have been dealt with at both the low and high levels of the design. This talk deals with approaches for improving dependability at the system level.

## Faults in CMOS ICs

The “stuck-at” model has been the dominant fault model for ICs. However, as technology advances, new trends including subwavelength lithography, random dopand fluctuations, hot-spots, and voltage variations, impact circuit behavior. “Delay fault” and “transient error” models more accurately capture the results of these trends in digital circuits. Non-idealities in scaled technologies also have a significant effect on analog and RF circuits, including matching problems, and effects on gain, linearity and noise figure.

The technology trends thus impact techniques for manufacturing test of ICs as well as on-line (concurrent) error detection techniques for systems.

## Testing systems on a chip

ICs need to be tested after manufacture to ensure that they are defect-free. Since each individual chip needs to be tested, the cost of testing a transistor does not scale with Moore's law, compared with the cost of its manufacture. Conventional testing is geared to detecting stuck faults using scan chains to access internal storage elements. Since delay faults are becoming more common, ICs need to be tested at speed. Techniques have been developed to use on-chip resources to run tests in native operating modes.

The technique of “native-mode self test”, which executes instruction sequences in order to detect faults in a processor, has been applied to manufacturing test of complex processors. Approaches have been developed to generate instruction sequences for a processor which will apply tests for path delay faults in internal modules.

The high level of integration possible with scaled technologies is enabling entire systems on a chip. The trend, driven by consumer electronics, is to include analog and RF modules in these chips. These modules have to be tested for compliance with their specifications. Techniques have been developed to use the embedded digital processors to test the analog and RF modules. One approach is to place the analog modules in loopback mode during the test, for example, a digital-to-analog converter feeding an analog to digital converter. Techniques have been developed for checking for the individual specifications of the converters from the results of the loopback test. One approach to test RF circuits for high-frequency specifications is to embed sensors on the chip, so that the specification can be predicted from low-frequency measurements, reducing the cost of test.

## Fault Tolerance

Dependable operation in the field requires techniques for detecting and correcting errors due to faults, as well as re-configuration around permanently failed units. High level techniques have been developed to check for the correct outputs of computation units as well as for the correct control flow in the system.

Simplistic approaches for redundant computations to detect errors require a high cost, for example, triplication and voting. The technique of “algorithm-based fault tolerance” encodes the data at a high level, so that errors can be detected and corrected with low overhead. This has been successfully applied to matrix operations.

Techniques have been proposed to check for correct control flow in a processor. Recently, these ideas have been integrated with the GNU compiler, gcc, so that code for detecting and correcting control flow errors can be automatically inserted in an application at compile time.

## Conclusions

The effects of faults in ICs at the transistor level on the system-level behavior can be exploited to develop efficient techniques for manufacturing test as well as for error detection during operation, enabling a high level of dependability with low cost.