

Quantitative Productivity Measurement in IC Design

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Abstract

This paper describes ongoing research in the field of quantitative productivity measurement in IC Design and simulation of different scenarios as decision support. Five topics out of this research field allow an insight in the preparation of real design flows for productivity measurement and how these measurements are used for analysis, simulation and optimization of design flows. This paper starts with an introduction in section 1 of the PRODUKTIV+ project in which most of the research has been done. The modeling of projects and extraction of the important indicators complexity and quality is explained in sections 2 and 3. In section 4 Synopsys as an EDA vendor from outside of PRODUKTIV+ adds its view on productivity measurement. Section 5 contributes to the modeling of a verification process for productivity simulations. Section 6 explains an optimization process for a microprocessor design flow under productivity considerations.

Most of this work has been carried out in the PRODUKTIV+ project (label 01 M 3077) that is partly funded by the German government [17].

1.1 Introduction: Turning EDA investments into productivity increase

You can't improve what you can't measure. So prior to being able to improve design productivity we have to make it measurable. Furthermore, the influence of all contributing factors to the resulting productivity needs to be understood and quantified.

Closing the well-known design gap requires a significant increase of productivity within IC design. Actual productivity has to be quantified as a solid base for project planning, project management and for improvement of development processes. In manufacturing, frequent updates of productivity indicators is a common procedure. In R&D, measuring productivity is not straightforward. The actual value of productivity is hard to quantify and often less objective. Decisions are strongly based on experience and 'gut feel'. Approaches to determine productivity within IC development projects are limited to post-mortem analysis and only cover the important influence of EDA tools and libraries implicitly.

PRODUKTIV+ target is a detailed quantitative measure, predictive estimation and simulation of design

productivity, yielding alternative scenarios for solid project management decisions. Especially, benefits of EDA investments will be quantified for proper investments to close the gap and safe-guard jobs.

PRODUKTIV+ is not limited to certain design types. It covers the whole spectrum of digital and mixed signal applications, including automotive, communication and microprocessor design.

1.2 Project Overview PRODUKTIV+

The project is subdivided into work packages with focus on

- **modeling:** A resulting ontology holds all relevant information on the components of a design system including relations between them. The model is powerful enough to describe the different design systems used by the current partners and expandable for partners joining later.
- **data gathering:** we provide tools and methods to gather data from current design projects. Focus has been set on high automation level thus reducing extra workload for engineers using the design system. Data sources include license usage, tool log files, versioning control log data as well as log data from computing resources.
- **simulation and analysis:** based on data collected during the previous step, the initial models will be calibrated to reflect the actual design process. Depending on the amount and quality of available data, we will use methods like Data Mining and Principal Component Analysis (PCA). The resulting models need to be verified against project data. Once a set of models is available, we can start simulation the design process. Currently, simulation approaches under evaluation are a simulation based on a Request Service Model as well as Multi Agent simulation. The simulation is one of the most powerful outputs of the project since it allows users to assess several scenarios (investment decisions, tool selection, Design Flow setup) before project start.
- **implementation:** all methods are implemented into the partner specific Design Flows

1.3 Results provided by PRODUKTIV+

After project completion, PRODUKTIV+ will provide

- the link between EDA investments and their productivity impact
- decision support by simulation of multiple scenarios (what if analysis)
- support in controlling
- inputs for benchmarking

The project consortium consists of AMD, Cadence, Infineon, Bosch, universities and research centers. In this

paper this introduction and the following sections 2, 3, 5 and 6 describe the scientific background as well as the implementation of methods during real projects. The topic will be complemented in section 4 by an EDA vendor's (Synopsys) viewpoint on productivity measurement.

2 Determining the Technical Complexity of Integrated Circuits

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2.1 Abstract

The classification and quantification of a projected design's technical properties is essential for the prediction of success or failure of a microelectronic development project. The derived values have to mirror the design's capacity and thus allow for an estimation of the design complexity. This chapter depicts the PRODUKTIV+ solution approach to the ascertainment of a design artifact and the determination of equations in particular.

2.2 The Design Project Character

In general, we defined the Design Artifact Complexity (DAC) as a business ratio within a business ratio system called Design Project Character (DPC [7]). As described in [4] and [7], the DPC is being build bottom up. Consequently it satisfies not only economic but also technical demands.

The DPC allows capturing a design project as a whole and therefore to react appropriately to possible bottlenecks beforehand. To enable this, a set of company and project specific parameters have to be acquired and imported into the calculation software. These parameters describe the general features of the design environment (EDA tools, designer, computing resources...) as well as the technical characteristics of the scheduled design.

2.3 Hierarchy

The DPC business ratios are calculated by the algorithmically linked ratios of the level beneath. The bottom level is composed of measurable parameters, while the top level consists of the following five ratios: Finances, Design Artifact Specifics, Resources, Human Resources and Design Flow. In principle, the DPC hierarchy is to be build based on a data mining method that detects correlations between parameters of real projects (conducted by our producing partners) and the corresponding target.

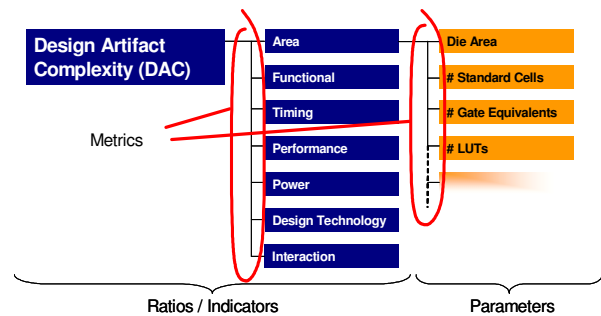


Figure 1: The Design Artifact Complexity as an excerpt of the DPC Hierarchy

In case of the DAC, this would be the development effort in man-days needed for the development of the design. The more complex a design, the more protracted is its development.

2.4 Next Steps

Due to the cooperation with three large semiconductor companies, the PRODUKTIV+ project has a good basis for the verification of this approach.

Through the access to these companies' data bases of future and already conducted projects, it should be possible to automatically generate the DAC metrics and align them via a control loop. For the generation of metrics data-mining methods are considered.

At present time, the available data sets are not sufficient. This is caused by the fact, that some defined parameters are not usually stored within the standard design flow of the partners. To deal with this, we are implementing some methods to decrease the necessary number of data sets – for example using the knowledge of experts.

3 Qualitative and Quantitative Analysis of IC Designs

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3.1 Motivation

A project's output needs to be quantified to enable the evaluation of its productivity. Besides complexity the quality of result is a main criterion to consider.

Based on the quality definition of "conformance to requirements" (see e.g. [14]), our approach combines requirements and quality modelling to allow real time tracking of the project status for integrated circuit design. Each design project has its individual (quality-) requirements and even components of the same design may differ in this aspect. A general quality evaluation

concept has to cover this individualism. A simple example is a component that should be reusable in multiple designs and therefore has to fulfil specific criteria ([11], [13]).

Our approach utilises a machine readable requirements definition in combination with common quality modelling techniques. Requirement fulfilment degrees and the current quality are computable based on this requirements definition and a snapshot of the current development status.

The Permeter framework developed by OFFIS is used to collect the data that represents the current development status. Permeter offers the functionality to load product data from different sources and establishes links between the data, e.g. requirements and corresponding components. Permeter offers both manual and (semi-) automatic linkage facilities. For a detailed description of the data integration process refer to [15].

3.2 Quality Criteria

There are three types of requirements that must be taken into account. First of all, the design has to be functional correct. Therefore, the fulfilment degree of each functional requirement based on the current verification status is an input factor for quality. Coverage metrics of different EDA tools have to be integrated to calculate the fulfilment degree of functional requirements. As mentioned in [16] it is mandatory to handle the vast amount of verification data from different sources to get an overall understanding of verification completeness. Loading these data into one format offers the possibility to achieve this goal. The aggregation of different verification coverage metrics into one single verification completeness value is a topic under research. Using the established data link between a function and its corresponding design component, the fulfilment degree of a functional requirement is determined through the verification completeness of that component. Furthermore, design constraints as area, power or temperature restrictions have to be evaluated. Even if the functional correctness is verified, the overall quality suffers from not meeting the physical design constraints.

Design constraints are modelled by a target value, a border (min/max) and a tolerance limit. These properties in combination with the current value establish a metric to assess an actual fulfilment degree.

Finally, non-functional quality requirements, like e.g. maintainability must be considered. We use the common technique from software quality modelling to break down complex quality indicators hierarchically into measurable parameters (e.g. [12]). After the aggregation of the measurable parameters to a result, it can be matched with a defined target value to assess a requirements fulfilment degree.

Ontologies are used to represent both the requirements as well as the metrics to assess the fulfilment of design constraints and non-functional quality requirements.

Requirements can be linked to the whole product, to a single component and to intermediate results, as e.g. the RTL Code (see [15]). This individually forms the quality criteria to be used in a quality evaluation.

Once the fulfilment degrees of requirements are calculated, they are used in combination with defined weights to assess an overall quality. The results will be displayed in reports to allow an easy detection of quality problems.

Future work will focus on the implementation of the concept and case studies with PRODUKTIV+ industry partners where different quality criteria and their dependencies are analysed.

4 Capturing and Analyzing IC Design Productivity Metrics

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4.1 Abstract

You can't improve what you can't measure and many people won't take the time to measure. This tutorial describes a practical, low impact method used by Synopsys Professional Services design teams to measure and analyze design flow and runtime metrics on their customer chip projects. Details about the capture methodology, database, and reporting infrastructure will be discussed. Uses for the metrics reports, as well as an overall context for design productivity improvement will be discussed. Although the details are provided within the framework of the Synopsys Design Environment, the concepts described are applicable to any structured design environment.

4.2 Synopsys

You can't improve what you can't measure and many people won't take the time to measure as this is regarded as a non-core activity to the business of SoC implementation. This is an unfortunate truism that prevents many SoC design teams from adopting a structured and methodical approach to Productivity Improvement. This tutorial describes a practical, low impact method used by Synopsys Professional Services design teams to measure and analyze design flow and runtime metrics on their customer chip projects. We start with a look at the definition of Productivity as well as some of the ideas that have been put forward as potential areas of improvement. Details about the capture methodology and the fundamental requirements of real time and low impact (low overhead and unobtrusive) collection are discussed. We also explore mechanisms to

store the information gathered, using an SQL-lite database in our case, and the need to be able to use the information stored. Generating information is not sufficient to improve productivity as in addition there needs to be a readily accessible and structured reporting mechanism in place. This should allow both micro and macro analysis and be applicable to both the current project and also for further strategic analysis and planning to move organizational productivity forward. In this case no distinction is made between human and infrastructure resources and data is gathered and analyzed from both groups. Uses for the metrics reports, as well as an overall context for design productivity improvement are then discussed. The details provided are within the framework of the Synopsys Design Environment and some time is spent to explore the details of the capture, storage and analysis of the data. The concepts described, however, are applicable to any structured design environment. Following the description of the productivity analysis environment the tutorial returns to a key theme, that of comparing and contrasting different projects. With every SoC design project unique how can we successfully compare two different projects and decide which project has been more productive. This thread is expanded to discuss normalization of disparate projects and finally the results of several years of systematic productivity improvements. The tutorial concludes that assessing IC design team productivity improvement is possible but that it requires careful definition and measurement along the way.

5 Application of Workflow Petri Nets to Modeling of Formal Verification Processes in Design Flow of Digital Integrated Circuits

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5.1 Abstract

According to statistics the verification of digital integrated circuits (IC) claims up to 70 % of the design time and effort in the design process. This means that the verification process must be well structured and organized in order to efficiently reach desired verification goals. This paper describes the modelling of an exhaustive formal verification process of a digital IC with Workflow Petri Nets [8] and the WoPeD (Workflow Petri net Designer) tool [9], which supports modelling, simulation and analysis of a workflow process. The purpose of this work is to formalize and quantify the verification process such that it could subsequently be structurally and behaviourally analyzed according to the means provided by Petri Nets and, if desired, simulated with a particular scenario. This approach makes it possible to explicitly

examine and derive the interaction of different factors which influence a verification process such that their relationships could be quantified. Initial experimental results are presented and advantages and disadvantages of this methodology are discussed.

5.2 Introduction

With the increase of the digital IC complexity the time and effort for their verification, needed to guarantee the quality and the safety of the product, rises disproportionately. To ensure the efficiency of the verification it must be well organized and structured. To achieve ambitious verification goals significant attention must be devoted to the verification management. The task of verification management is not only to produce well structured verification plan but also to control the entire process flow.

In this work an existing digital IC verification flow based on formal verification techniques (e.g. model checking) [10] was documented. The verification flow consists of six processes: verification management, verification environment, implementation and benchmarking of formal properties, verification execution, debugging, quantification and analysis. The possible factors of influence on the flow are: verification goals, circuit's complexity and resources. For different verification goals the processes *verification management* and *quantification and analysis* are different. The more complex the design under verification (DUV) is, the more involved is the verification management and the corresponding verification plan. This, in turn, has an influence on the complexity of formal properties, the size of the property set, and also on the choice for an appropriate verification environment. The available resources have an influence on the feasibility of the verification task and on the verification management. The aim of this work was to develop a model which would explicitly show the interdependency of different influence factors and provide assistance in choosing an appropriate workflow by considering restrictions and goals. Furthermore, to be able to control this flow a formal and dynamic model is needed. This model should represent the flow of activity and should be executable under the influence of certain criteria, factors and current status data. This work describes the first experiences in modelling a formal verification process using Workflow Petri Nets [8].

5.3 Approach & Experience

The purpose of this work was to convert the conceived verification process originally documented as a static process flow captured in flowcharts into a hierarchical formal representation. The Workflow Nets, an extended class of Petri nets, are appropriate for this task. The tool

used was WoPeD [9], which supports modelling, simulation and analysis of workflow processes and resources descriptions using workflow nets.

The investigations show that the development of a complex, hierarchical and closed-to-reality model is a challenging task. Due to tool limitations some of the hierarchy blocks of the model had to be flattened. However, the flattening caused unmanageable model; therefore, it had to be simplified. In the end, a formal model of a simplified verification flow was created. It was possible to perform structural and behavioural analysis, simulation and even capacity planning on the modelled workflow net. However, the capacity planning has so far only one resource included - the time.

The advantage of the presented approach is the ability to capture a verification process with an executable model which allows static and dynamic analyses. However, there are challenges regarding support of hierarchical flows and capacity planning which are currently being addressed.

6 Optimization of Design Flows for Multi-Core x86 Microprocessors in 45 and 32nm Technologies under Productivity Considerations

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6.1 Motivation

Designing next generation 45nm and 32nm multi-core microprocessors creates new challenges caused by a dramatic increase of design complexity and constraints such as:

- increasing number of cores per chip
- enhancing cache sizes and cache systems
- increasing frequency for memory and serial interfaces
- heterogeneous multi-core architectures
- functional enhancements (security, virtualization, ...)
- DfY/DfM/DfV require the consideration of more and new technology specific characteristics.

Without a considerable improvement of design productivity new products will not be available in time to market to create maximum economic value.

The presentation describes how an infrastructure to measure productivity relevant parameter for a microprocessor design flow for 45 and 32nm technologies can be build up.

6.2 Objectives

In order to develop a proper infrastructure for productivity measurement the objectives for the productivity analysis

need to be defined. Within the AMD design environment the following objectives were identified:


- Identify areas for productivity improvement
- Root cause existing productivity weaknesses.
- Provide benchmarking capabilities to measure the level of improvement after a design flow optimization
- Create a knowledge base to improve the planning quality for new projects

As mentioned the before all those objectives are indented to support a competitive time-to-market for microprocessor products.

6.3 Approach & Experience

Based on the concepts developed in PRODUKTIV+ a largely automated environment was implemented to determine a so-called “tape-out-readiness” indicator. This infrastructure is used as a first vehicle to prove the feasibility of the proposed methodologies and approaches. It tracks the convergence of design quality criteria that are crucial to successfully tape-out a 45nm multi-core microprocessor design. Currently more than 50 tape-out relevant quality criteria (such as timing, DRC, LVS, IR drop, electromigration and others) are captured in a database environment and visualized in a web-based environment. The actual status of those parameters for each sub-block of the microprocessor design will be aggregated by an algorithm to a single indicator showing the convergence to a design quality needed for tape-out. Figure 2 gives an example for possible aggregation function for a subset of quality criteria. This indicator is getting tracked over time for all blocks.

Criteria	Function	Criteria	Function
LVS-status	$f_1(x) = \begin{cases} 1, & \text{if } x = \text{clean} \\ 0, & \text{else} \end{cases}$	Criteria 7	$f_7(x) = e^{-\frac{x}{3}}$
DRC-status	$f_2(x) = \begin{cases} 1, & \text{if } x = \text{clean} \\ 0, & \text{else} \end{cases}$	Criteria 8	$f_8(x) = e^{-\frac{x}{3}}$
Noise violation	$f_3(x) = e^{-\frac{x}{20}}$	Criteria 9	$f_9(x) = e^{-\frac{x}{10}}$
Criteria 4	$f_4(x) = e^{-\frac{\text{bucket} + x}{10}}$	Criteria 10	$f_{10}(x) = e^{-\frac{x}{3}}$
Criteria 5	$f_5(x) = e^{-\frac{\text{bucket} + x}{10}}$	Criteria 11	$f_{11}(x) = e^{-\frac{x}{20}}$
Criteria 6	$f_6(x) = \frac{\text{bucket} + 3}{\sum_{i=1}^n \text{buckets}}$	Criteria 12	$f_{12}(x) = e^{-\frac{x}{10}}$



$$F_{Indicator} = \frac{\sum_{i=1}^{12} f_i}{12}$$

Figure 2: Example for aggregation function

The analysis of this indicator is used to quickly identify issues in the convergence of the design quality and take appropriate counter measures addressing the problem identified immediately rather than after a few days. This capability is specifically important because it can automatically highlight issues real-time in large cross-site design teams working in different time zones worldwide. Figure 3 shows an example for a tape-out-readiness trend

chart for a single block of a microprocessor design including various trend lines.

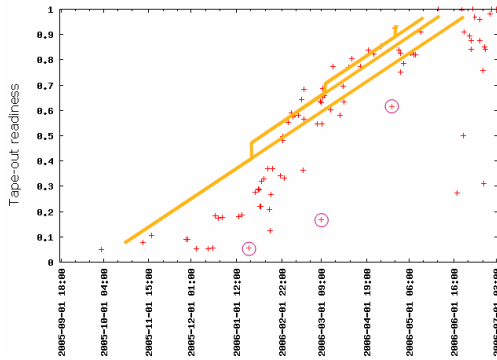


Figure 3: Chart for tape-out-readiness indicator including trend lines

As a next step besides optimizing the implementation flow a similar approach is under development for the functional verification of microprocessor designs.

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