A Programmable and Low-EMI Integrated Half-Bridge Driver in BCD Technology

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Abstract

This paper presents the design and the laboratory results of an integrated half-bridge driver for power electronic systems in a 0.35 µm Bipolar CMOS DMOS (BCD) technology. The proposed solution is designed for frequency applications up to several hundred of KHz and it has a driving current capability up to 50 mA. This work features a design configuration and a digital control to reduce electromagnetic interference (EMI). Moreover it includes short circuit protection, programmability of voltage references and a digital control circuitry implementing mechanism to prevent dangerous failures of the driver. After a deep description of the circuit we show the laboratory results of the half-bridge driver used to drive a 20 KHz antenna.

I. Introduction

The design of MOS gate drivers plays a key role in the overall quality of a power electronic application such as motor driving, power converters or antenna driving. The trend of the last years is to move from discrete circuits with big and expansive components to fully integrated circuits. System integration opens certainly the way to new important advantages. Area occupation is probably the most important features together with cost reduction, but also a higher level of reliability is possible to be achieved since control and protection features are easier to be implemented in a single chip solution [1, 2].

Numerous papers have been published in recent years on different integrated solutions to implement gate drivers operating at various operating frequencies and with different power devices [3, 4, 5]. All the proposed designs focus on area and power consumption saving without any particular care to EMI that represents a key point in the specification of many power electronic products.

In this paper we present the design of an integrated gate driver for a power inverter connected to a supply voltage up to 40 V. The system has been integrated in a 0.35 µm Bipolar CMOS DMOS (BCD) process supplied by STMicroelectronics. The proposed solution features a complete programmability and control of turn on and turn off current capability in order to reduce EMI and limit the dv/dt of power MOSs drain. Furthermore this solution includes short circuit protection and a programmable voltage reference to set the DC value of the gate-to-source voltage (V_{GS}).

In section II and III we describe the functionality of the analog circuit focusing on the schematic of the adopted solution. In section IV we present the digital section of the structure. In that part we focus on the control circuitry implemented, underlying the potential failures and the mechanisms adopted to prevent them. Finally we show the results of laboratory tests over a particular configuration and then we draw the conclusions.

II. Gate Drivers

Soft switching commutations of external power devices becomes crucial in applications where low-EMI is a must (e.g. antenna driving) and in applications where power stages drive inductive loads thus having to manage with high stored energies. The turn-on and turn-off characteristics of MOSs are both determined by the total gate charge (Q_G) of the MOS that is typically defined as the charge to be supplied to the gate to switch on the MOS in a particular circuit configuration. The total charge to be delivered depends on the gate-to-source (C_{gs}) capacitance and on the gate-to-drain (C_{gd}) capacitance. C_{gd} typically requires more charge than C_{gs} due to Miller effect. Moreover Q_G is strongly dependent by the drain current and drain-to-source voltage to be managed by the power MOS.

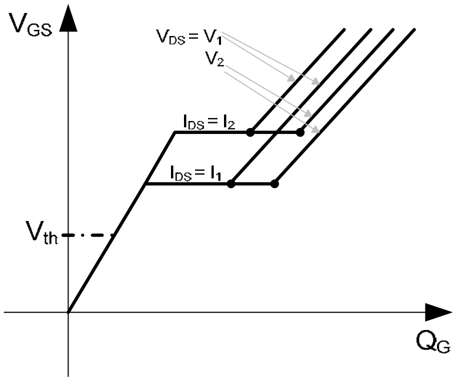

Figure 1. Gate-charge (Q_G) versus gate-to-source voltage (V_{GS})

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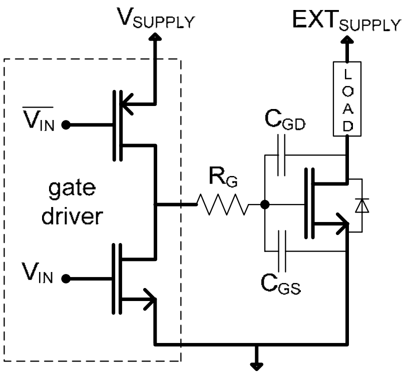

Figure 2. Simplified diagram of a typical gate driver

In figure 1 is shown the typical relationship between V_{GS} and Q_G of a power MOS driven by a constant gate-current.

The first voltage rise can be divided in two different phase. The first one represents the charging of C_{GS} up to the threshold voltage (V_{TH}) of the power MOS. In the second one V_{GS} continues to rise while the drain current begins to increase up to the value fixed by the circuit. The flat portion, called plateau Miller, represents the discharging of the Miller capacitance related to C_{GD}. The second rise is additional charge which is not relevant to switch on the MOS but mandatory to reach the DC V_{GS} value that determines the ON resistance (R_{ON}). It is important to notice that the drain voltage transitions take place during the flat portion when the voltage of drain-plate of C_{GD} is pulled down to the source voltage [6].

Typical gate drivers are realized with a push-pull stage driven by a digital control signal V_{IN} as sketched in figure 2 [7, 8]. When the gate is turned on or off, the push-pull stage provides a large current thus reducing significantly switching times. However, fast gate switching could easily lead to fast transition of the drain potential therefore increasing significantly EMI. Moreover fast transition of drain voltage could be capacitive coupled inside the driver causing undesired gate voltage switching. It is not unusual in power applications to have voltage spikes that could turn on the power MOS or at the opposite could cause underground gate transition thus leading to the injection of huge current in the substrate of the driver circuit.

An intelligent and simply solution to introduce soft gate-switching commutation and reduce EMI is to implement a mirror configuration to supply a programmable current I_G during gate charging interval (Figure 3). In a first approximation we can consider that a constant current is supplied to the gate, so the horizontal axis in figure 1 representing Q_G is directly proportional to the current I_G supplied to the gate. Therefore, programmability of I_G allows the user to increase or reduce switching time intervals accordingly to system specifications in terms of frequency switching and EMI. Time to switch on/off the gate MOS is approximately:

$$t = Q_G / I_G \qquad (1)$$

where Q_G is a design parameter related to the target DC V_{GS} to be reached.

III. Mirror Configuration Gate Driver

The schematic of the integrated driver is depicted in figure 3. The proposed solution has been designed to drive an external power half-bridge (Nch-MOS and Pch-MOS) with a typical operating voltage of 12V (VBATT) but it is able to drive circuits connected to a supply up to 40 V. This architecture is intended to work in the range of low frequencies (up to hundreds of KHz) with a maximum

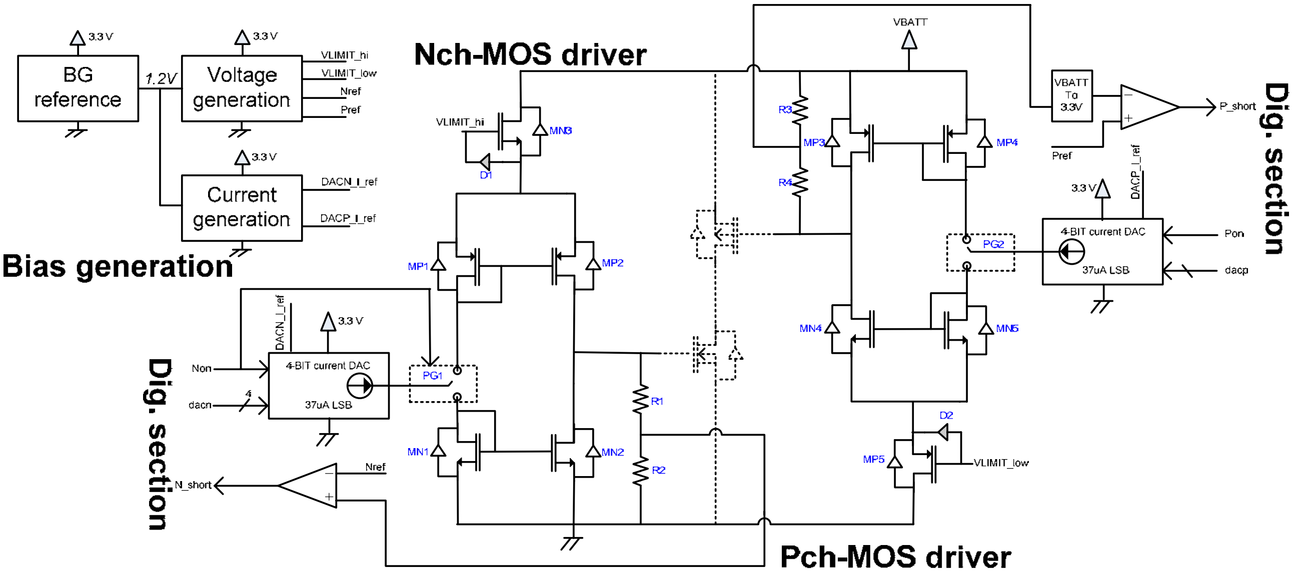

Figure 3. Half -bridge driver schematic

driving current capability of 50 mA. The circuit can be divided in two main sections: the first is the Pch-MOS driver and the second is the Nch-MOS driver. The voltage supply of the low voltage section of the two drivers is 3.3V as shown in figure 3. Each of the two driving sections is composed by a 4-bit current DAC with an LSB of 37 µA. The DACs use a bandgap derived current to achieve power consumption stable over temperature. The output DAC current is sent to the output push-pull driver stage by means of digitally controlled pass-gate (PG1 and PG2) in order to activate low-side or high-side of each driver. The digital section proposed to properly program DACs will be described in the next section.

For simplicity the push-pull stage is the same for each of the two drivers. It has been designed using high voltage devices supplied by BCD6 technology in order to manage the external voltage supply of 40V: for this reason NDMOS and P-ch rain extension MOSs with a drain-to-source voltage capability of 50 V have been chosen. The ratio of the mirrors MN1/MN2, MP1/MP2, MN4/MN5 and MP3/MP4 have been fixed to 1/85 thus the LSB current DAC is increased to 3.145 mA and the maximum current deliverable by the driver is 50.3 mA. The mirror ratio together with electro-migration requirement, have fixed the size of each MOS of the push pull stage (MN2, MN4, MP2, MP3) at about 0.012 mm^2.

The pass gates PG1 and PG2 shown in figure 3 are used to activate/deactivate low-side and high-side of each driver in order to alternatively turn on and turn off the external MOS. They have been designed using 3.3V devices and they are driven by a Pulse Width Modulation (PWM) signal generated by the digital section. This solution allows the driver user to get high flexibility in terms of half-bridge frequency operation and in terms of duty cycle.

The Pch push-pull stage works between VBATT and a programmable low-level voltage reference, while the Nch one works between a programmable high-level voltage reference and ground. These two references are generated by two high voltage source followers (MP3 and MN5) whose size have been chosen to guarantee power reliability and fast voltage recovery during switching transitions. The gate voltage references for the two source followers are derived by a bandgap reference as shown in figure 3. The high voltage reference can be set between 4V and 10V, while the low voltage one can be set between (VBAT-4)V and (VBAT-10)V thus allowing the user to set the value of the DC V_{GS} of the external Nch and Pch MOSs and therefore the value of Q_G and R_{ON} of the external half bridge. This is an important feature since many applications require low R_{ON} and depending on the characteristics of power MOSs, V_{TH} could vary significantly.

After the explanation of the proposed driver, we can introduce the functionality: during the Nch gate turn-off phase the low-side of its driver is activated and it sinks a current fixed by the DAC until the external device is completely turned-off. The current sank by the high side is negligible in this phase since it is supplied by a current 100 times lower. During the Nch gate turn-on phase the high-side is activated sourcing a current fixed by the DAC until it is completely switched on. In this case the gate reaches the DC value fixed by the aforementioned programmable voltage reference. Moreover the current sank by the low-side is negligible and doesn't affect significantly gate switching since it is supplied by a current 100 times lower. For the Pch driver the behavior is the same. It is important to notice that during the operating condition of this driver, it is not required any kind of level shifter to drive MP2 and MP3 since the gate are driven recurring to the proposed mirror configuration.

The total amount of power loss of the driver is determined by five main factors: the value of the equivalent capacitance C_{IN} of the MOS that fixes the amount of charge Q_G to be delivered, the value of the DC V_{GS} of external MOSs, the switching frequency f_S, the on-resistance R_{ON} of the driving transistors MN2, MN4, MP2 and MP3 and the current I delivered by the driver:

$$P_{TOT} = C_{IN} \cdot V_{GS}{}^2 \cdot f_S + R_{ON} \cdot I^2 \cdot \left(\frac{T_{ON} + T_{OFF}}{T_S} \right) \qquad (2)$$

The DC supply current of the driver is divided between the low voltage and the high voltage section. Depending on the configuration of the current DAC, the 3.3V supply delivers from0.3 to 2.7 mA, while the high voltage supply delivers from 1.3 to 4.6 mA. During the transient the power consumption of the high voltage section arises accordingly to equation 2.

The analog section is provided with a short circuit protection that prevents the source followers, generating voltage references for the push-pull stages, to be damaged and that automatically turn off the whole gate driver after short detection. In fact MOSs used in this design have all a 3.6V gate-to-source maximum voltage capability in operating conditions, thus the circuit must guarantee that this limit is never exceeded during circuit lifetime. The proposed protection consists in a simple diode between gate and source (D1 and D2) as shown in figure 3. Referring to the Nch driver, if the Nch gate is shorted to VBATT, without the protection diode, V_{GS} of the source follower would be biased at a high reverse value, leading to a fast degradation of the gate oxide. The insertion of the diode allows V_{GS} to be clamped at about -0.8V thus saving the gate-oxide. During normal operating conditions or ground short circuit, which is not dangerous for the integrity of the gate driver, the diode is reverse biased and doesn't affect the behavior of the circuit.

The two drivers are provided with a pull-down (R1 and R2) and a pull up (R3 and R4) resistor to switch off the external gates when the driver is OFF. Moreover when the half-bridge driver is on, these resistors are used to sense the gate of the external MOS. If after a half period of PWM driving signal the gate has not yet switched to the expected value, the digital section generates an interrupt, stops the communication and power down all the driver blocks. This digital short detection is active for both ground and VBATT short circuit.

Finally this design is provided with power down circuitry (not shown in figure 3 for simplicity) in order to reduce as much as possible power consumption when the driver is not used. This is very useful when the driver is integrated in a chip together with other analog IPs since the power consumption can be dramatically reduced when this block is not used.

IV. Digital Control of the HV Driver

The half-bridge driver has two driving sections, each one is composed by a 4-bit current DAC. The digital driving of these DACs must be designed with particular care in order to couple low area occupancy, reliability, low EMI and protection from short circuits.

In figure 4 is depicted the block diagram of the HV driver including the digital driving section.

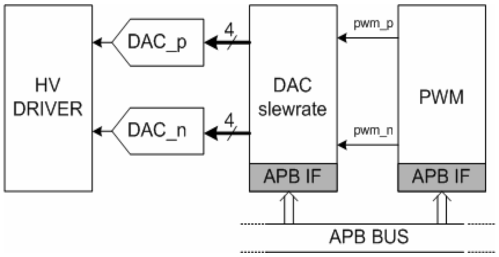

Figure 4. Block diagram of digital controller

PWM generator and DAC_slewrate, shown in figure 4, are specifically designed for the driving of the HV driver. Both have an Advanced Peripheral Bus (APB) interface that grants fully access and programmability from an APB-compliant CPU.

The PWM generates two signals for every driver, one for the Nch gate and one for the Pch gate. It consists in a common prescaler register plus a programmable 8-bit up-down counter for every driver. The programmability of this counter allows the user to set the prescaler and the maximum value (PWM_max) of the counter, that directly affect the wave period and the PWM threshold value (PWM_comp) that affects the duty cycle of the wave.

Every counter generates two waves using the same value of PWM_max and PWM_comp, in this way both signals have the same behavior. The PWM output is depicted in figure 5. The behavior of the signals shows clearly that the pwm_n and pwm_p signals can not be overlapped. This is a required feature for this design: in this way the designers grant that a cross conduction between external power MOSs can not be generated.

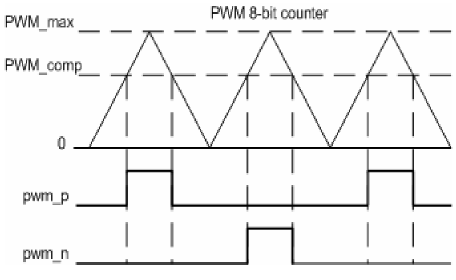

Figure 5. PWM output signals behavior

When PWM counter reaches PWM_max or zero the device can generate an IRQ to alert the CPU. At the same time the information about what type of event occurred is stored in a status register. Obviously this IRQ generation can be masked if not needed for the application.

The minimum PWM frequency that can be reached is:

$$f_{\min} = \frac{f_{clk}}{((\mathrm{PWM\_max}+1)(\mathrm{prescaler}+1))} \quad (3)$$

that means for a 16 MHz clock and a 2-bit prescaler a minimum frequency of 15625 Hz.

The duty cycle of the generated signal can be calculated as:

$$\delta = \frac{(\mathrm{PWM\_max} - \mathrm{PWM\_comp})}{(2 * \mathrm{PWM\_max})} \quad (4)$$

with $0 \leq \mathrm{PWM\_comp} \leq \mathrm{PWM\_max}$.

The duty cycle can be set from 0% (PWM_comp = PWM_max) to 50 % (PWM_comp = 0).

The PWM guarantees that no overlap is possible for the two signals pwm_n and pwm_p, on the other hand it can not help the designer to have a low EMI. The better way to have a low EMI is to use a soft gate-switching that limit the dv/dt of power MOSs drain. In order to achieve this result a DAC_slewrate IP is designed.

The purpose of this device is to transform the PWM input signals in low-EMI signals reshaping their slopes. In fact these signals are the ones programming the current DAC and consequently they fix the external MOSs switching times. For every PWM output four 8x4bit Look Up Tables (LUTs) are implemented, two for every channel, one for the rise and one for the falling transition. Through one APB write operation the CPU can program a LUT: when an input rising edge is detected the output

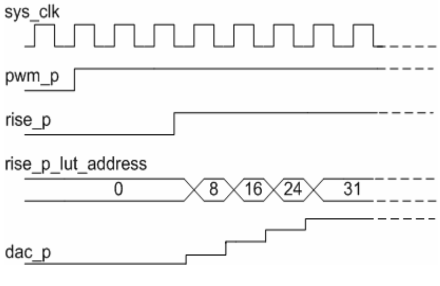

Figure 6. DAC_slewrate output timing

follows the LUT content, in this way the user can fix the maximum DAC value and the slope of the output signal. The scan time of the LUT can be programmed through a control register from 4 to 32 clock cycle for a complete rise (or falling). In figure 6 is shown the timing of the input and output signals for a 4-clock rise transition.

Due to the programmability of the LUT the user can find the right trade-off between low EMI and fast transitions, depending on the requirements of the target application. The risk of cross conduction is not completely avoided with the PWM generator, since a delay of the rising and falling edge of the output signals pwm_p and pwm_n can happen. To overcome this problem an internal signal delayer is provided. This delayer handles the output signals, if one input rise before the other one has complete its falling the related output will be delayed until a certain amount of time has passed. This amount of time can be programmed by the CPU depending on the application. Together with the signals for the DACs this IP also generates the signals for the pass-gates (shown in figure 3), in this way all the signals are synchronous with system clock.

The high programmability of these two IPs allows the user a great control over the waveforms that handles the half-bridge driver, thus featuring enhanced flexibility. Great effort has been spent to realize the safety mechanisms in order to avoid short circuits and to reduce the EMI as lower as possible.

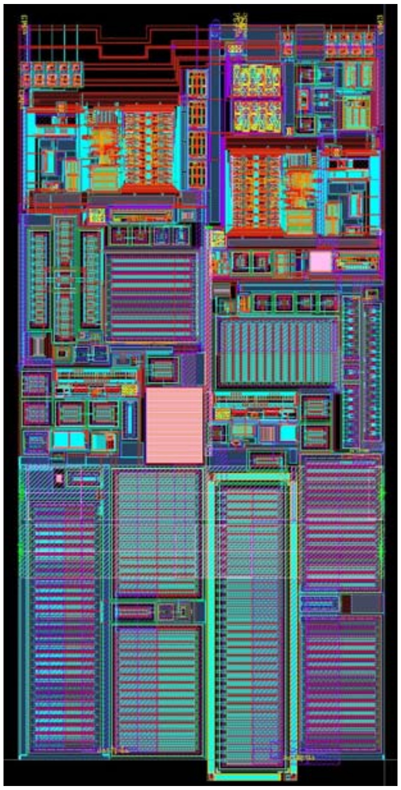

Figure 7. Layout of the half-bridge driver

V. Gate Driver Layout

The half-bridge driver has been designed using a 0.35 um BCD STMicroelectronics technology (BCD6). The layout is sketched in figure 7 where it can be easily distinguished the push pull HV driving stage within its voltage reference section that occupies a relevant part of the overall area. The upper side of the layout is mainly composed by low voltage circuitry (DAC, logic, biasing circuits) and by level shifters necessary to power down the HV section when it is unused or after a short detection.

The driver has been integrated with other analog IPs and with a digital core containing the aforementioned digital control section in a single chip. The total area occupied by the half-bridge driver is 1.05 mm^2 while the digital control section is 0.25 mm^2.

VI. Simulations & Measurements

The proposed solutions have been simulated using a particular circuit condition. The external half-bridge has been realized using IRF7309 Pch & Nch devices [9] with a voltage supply between 7V and 40V. Its output has been connected to a 20 KHz antenna. This test bench has been used to validate and characterize the driver and then it has been replicated in laboratory to measure real performances of the system.

In order to evaluate the real performances of the proposed solution in terms of EMI, two different driving current capabilities have been chosen. Figure 8 shows the gate-to-source voltage transition of the P-ch IRF7309 MOS during the turn on phase and the consequent drain node voltage transition, for the maximum driving current (about 50 mA). In figure 9 the same waveforms for a current capability of only 6 mA are drawn. It is immediately clear that with a strong reduction of the current it is possible to increase the time length of the plateau Miller from 114 ns to 632 ns thus decreasing the dv/dt of the drain voltage and consequently reducing significantly EMI. Furthermore with the minimum current

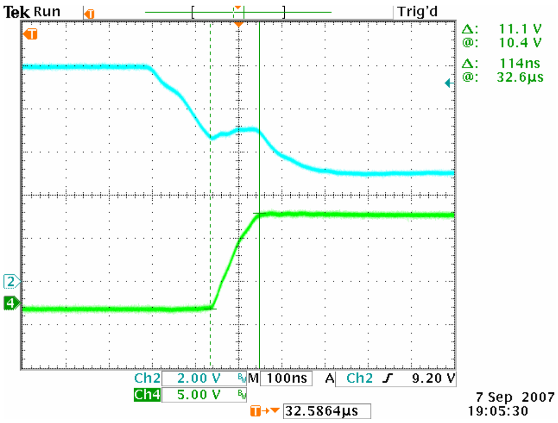

Figure 8. Fast transition of the half-bridge

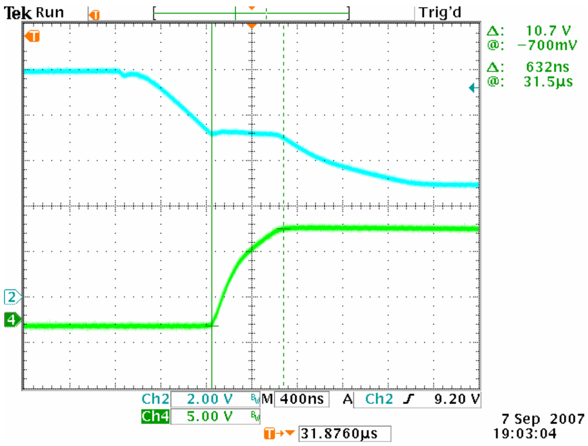

Figure 9. Slow transition of the half-bridge

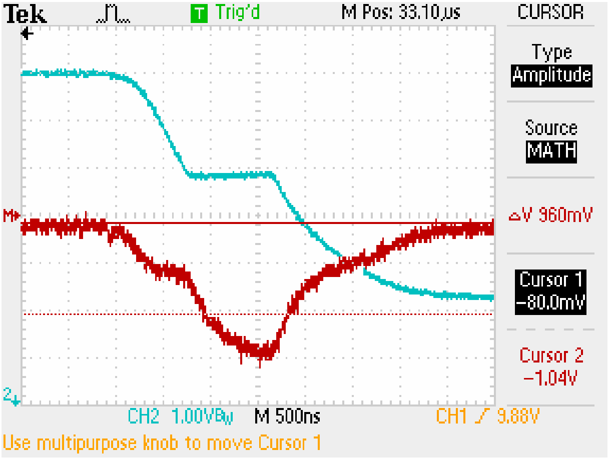

Figure 10. Current delivered by the driver to the IRF7309 Pch gate and IRF7309 Pch V_{GS} transition

capability of about 3 mA the plateau Miller time length is increased up to about 900 ns. Another important advantage of programming a low current capability is that the softer is the drain node transition, the lower is the energy stored in the antenna that has to be managed by the driver.

In this laboratory test both currents guarantee a very low turn on time of the Pch MOS if compared to the period of the PWM signal that is 50 µs: for the fast transition the turn on time is 400 ns, while for the slow transition is 2.4 µs.

Figure 10 shows in red the voltage across a 250 ohm resistance placed in series of the external gate, to evaluate the current delivered during the turn on phase from the gate driver in the case of 6mA current capability. It is important to notice that in the real condition the current is not constant over all this time as theoretically expected. In fact in the transient this current is shaped depending on the characteristic of the external gate and there is also shoot-through current going through both PMOS and NMOS driving transistors, but in any case it never exceeds the limit fixed by the DAC.

VII. Conclusions

The proposed half-bridge driver topology integrated in a 0.35 µm BCD technology, guarantees low-EMI thanks to the mirror configuration solution and thanks to the high level of programmability.

The circuit has been tested with an external power inverter using IRF7309 Pch and Nch MOSs. The measurements show that the time length of the plateau Miller region during turn on and turn off period of the external gate can be programmed between 114 ns and 900 ns thus leading to EMI reduction. During the overall gate transition time, the current delivered from the gate driver never exceeds the limit fixed by the 4 bit current DAC.

The half-bridge driver features a digital control to prevent possible and typical gate driver failures such as short circuit to voltage supply or ground and cross conduction between external power MOSs. The circuit is also provided with a power down circuitry that guarantees negligible power consumption when the block is not used. The proposed solution is intended to interface half-bridges supplied to an external voltage ranging from 7 V to 40 V and it can be used in applications with frequencies from 16 KHz up to several hundred of KHz.

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