

An Analog On-Chip Adaptive Body Bias Calibration for Reducing Mismatches in Transistor Pairs

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Abstract

Device parameter variations exhibit an increasingly serious impact on analog and mixed-signal circuit behavior. In this paper, we propose a novel fully-analog on-chip adaptive body bias calibration method, for efficiently reducing mismatches in transistor pairs. We present three circuit implementations which achieve a mismatch reduction between 61% and 73% in terms of standard deviation.

1. Introduction

On-chip analog and mixed-signal circuits for measurements, testing, and signal processing are significantly affected by device parameter variability, causing deviations of their output results from the correct value. One of the most important cause for such deviations is the device mismatch which occurs through process variations. In this work, we propose a new and efficient method to improve the performance of these circuits by calibrating the matched transistor pairs through an analog adaptive body biasing (ABB) circuit, which targets the reduction of the mismatch in the current-voltage characteristics of the matched transistors.

The paper is organized as follows. A theoretical background on prior ABB-based design methods and a concise summary of device variability compensation are given in Sec. 2. The proposed ABB calibration method is introduced in Sec. 3, while the three different circuit realizations and the implementation results are presented in detail in Sec. 4. Sec. 5 concludes the work.

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2. Theoretical Background

2.1. Prior Work on ABB

For the calibration of digital circuits, several voltage keeping [10, 11] and body biasing [9, 13, 14, 16, 18] approaches exist. However, these methods only target frequency increases and reductions in leakage, delay, and power, thus being of less interest for directly matching transistor pairs in analog and mixed-signal circuits.

For instance, [18] uses adaptive body biasing in digital circuits for increasing frequency and reducing leakage. In [11], a speed improvement and reduced delay variations in dynamic logic digital circuits are achieved through the use of a voltage keeper. A voltage keeper was employed in [10] as well, controlled by a current sensor that detects leakage variations. The authors of [16] target the reduction of dynamic power, leakage power, and increase in the speed of digital circuits by means of process variations estimation circuits and demonstrate a digital on-chip controller for selecting an *a priori* stored body bias value. A forward body bias is used in [13] for reducing delay variations in digital circuits and an automatic body biasing architecture for minimizing the active power consumption has been published in [9]. The approach in [14] employs only a fixed forward body bias after performing external measurements, not realized with an on-chip adaptive circuit.

In contrast with the previously-published work, our method employs an on-chip analog circuit and reduces significantly the current-voltage mismatches in MOS transistor pairs through an adaptive body bias adjustment.

2.2. Device Variability Compensation

As CMOS technologies scale toward 45 nm and beyond, an increasingly higher level of systematic and random variations in process, supply voltage, and temperature continuously affect the performance of integrated circuits [3–5].

and generates the corresponding rail-level signals for the subsequent charge pump (CP) circuit, according to the bias decision. The two charge pumps control the body bias levels by charging or discharging the capacitors connected to the transistor bulks. The two transistors can be either PMOS (in separate n-wells) or NMOS (in a triple-well process).

When a mismatch is sensed, the BDC blocks command a simultaneous body bias shift in opposing directions for the two transistors. While the body bias of one transistor might reach the limit of a supply level (e.g. 0 V for NMOS or V_{dd} for PMOS) during a correction, the correction can still be performed by adjusting the body bias of the other transistor, in the opposing direction.

For instance, let us assume a pair of PMOS transistors and a mismatch such that the current through the left-hand side transistor is lower, for the same bias conditions. In this case, the body bias decision states that the left transistor requires a higher V_B (a lower V_{SB} bias) for reducing its $|V_T|$ and, correspondingly, to increase its drain current. If $V_B = V_{dd}$, it cannot be further increased without having a higher supply voltage for the charge pump. However, the correction can still be performed, by lowering the V_B of the transistor on the right-hand side. This opposing bias decision principle is implemented in the BDC circuit.

4. Experimental Results

In this section we present three circuits that implement the analog adaptive body bias for matching the transistor pairs in an NMOS differential pair with PMOS current mirror load. Differential pairs and current mirrors count to the most frequent examples of matched transistor pairs employed in analog and mixed-signal designs. Each of the three circuits presented here achieves a substantial mismatch reduction for the entire differential stage, with slightly different performances. The decision to implement either one or another depends on the circuit size and on the desired correction accuracy. The correction performance of each circuit is evaluated here as the quantitative improvement in standard deviation of the output voltage mismatch.

4.1. PMOS Analog ABB Circuit

The analog ABB circuit with PMOS body biasing designed for the calibration of a CMOS differential stage is presented in Fig. 2. In this configuration, the PMOS transistor pair has the bodies connected to the ABB circuit. This is the most convenient circuit implementation, in which only the PMOS transistors are individually biased, since it does not require a triple-well process.

The mismatches in both the PMOS pair and the source-coupled NMOS differential pair translate into a voltage mismatch at the output of the stage, when a common-mode

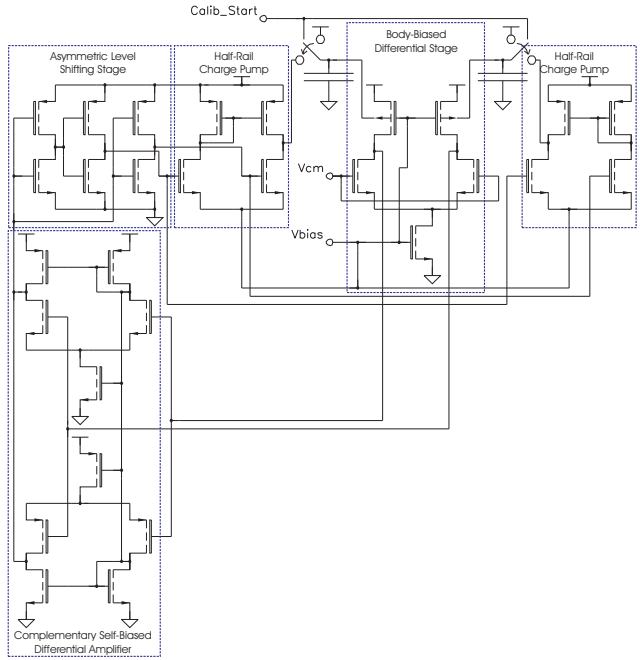


Figure 2. PMOS analog ABB circuit.

voltage V_{cm} is applied at the input. The differential output voltage resulted through mismatches is sensed and amplified by a comparator.

We have designed a high-gain rail-to-rail comparator by connecting together two complementary differential amplifiers with current mirror load and by providing a common internal bias node for the current sources. The idea is similar to the one published in [2], where two source-connected differential stages and two folded-cascode differential amplifiers are connected, after partially cutting down the load. Here, we have connected two differential stages in a different way, and without cutting out the load, which enabled us to obtain a rail-to-rail differential amplifier with less transistors than the folded cascode from [2]. The obtained circuit allows us to accurately sense voltage mismatches with a common mode ranging across the entire rail-to-rail voltage span with a minimum transistor count.

The bias decision and control circuit is implemented here with a two-branch, asymmetrical level shifter. In order to ensure a full charging of the bias capacitors up to V_{dd} , and a complete cut-off of the discharging current after setting the body bias, the BDC block must provide supply-level voltages to the charge pump (i.e. clean V_{dd} or ground levels).

A level shifter is the most compact choice for performing the required tasks. Moreover, the level shifter must be asymmetrical, in order to correctly implement the bias decision. For instance, if the comparator output is at $V_{dd}/2$, meaning that the differential stage is perfectly matched, the level shifter must set both outputs on 0 V. When the com-

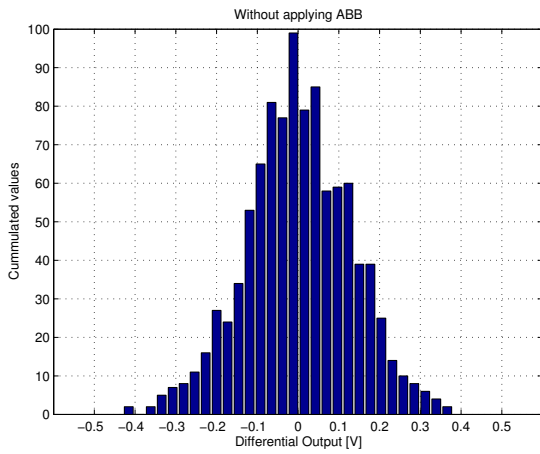


Figure 3. Distribution of the differential output without applying any correction.

parator output is at e.g. $25\% V_{dd}$, the non-inverted output of the shifter should be on 0 V , while the inverted output should already switch to V_{dd} , indicating to the charge pump that the left-hand side bias should be reduced and the right-hand side increased. Similarly, at $75\% V_{dd}$, the non-inverted output should be switched to V_{dd} , to command the charging of the left-hand side capacitor. In order to provide this asymmetrical behavior, the level shifter is designed to switch the non-inverting output at an input voltage higher than $V_{dd}/2$, and the inverting output at an input lower than $V_{dd}/2$.

The charge pump is implemented as a differential, source-coupled NMOS stage with PMOS mirror load, which ensures a full charging of the capacitor up to the supply level, with the minimum transistor count. A design novelty here is the reuse of the current source between the two charge pumps and the connection of the common-source node to an external bias point, fixed at V_{bias} . In this way, a half-rail swing is constrained, which ensures a moderate body bias, limited to about $V_{dd}/2$. The common current source for the two charge pumps and the voltage source V_{bias} are attached to the same node and not shown here for simplicity. The same is true for the schematics that follow. Experimental observations have shown that the forward body bias correction achieves its optimum at about $V_{dd}/2$ [4], which imposes the corresponding half-rail limit for the charge pumps.

We have simulated the circuit from Fig. 2 with Spectre, using a 90-nm, 1.0-V CMOS technology from Infineon, with accurate process variations obtained from the technology provider. In this way, all the transistors (differential stage and ABB calibration circuit) have been affected by process variations during the simulations. We have measured the voltage difference at the output, resulting from

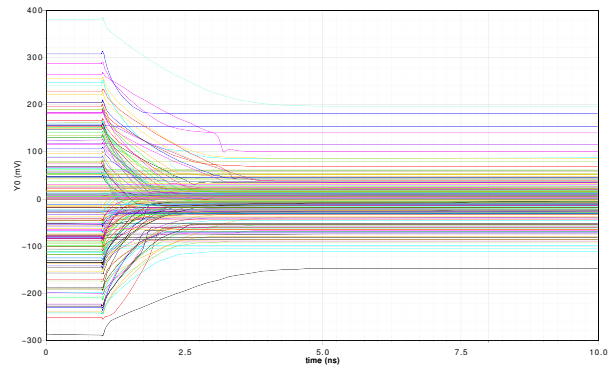


Figure 4. Differential output of the stage with PMOS analog ABB correction.

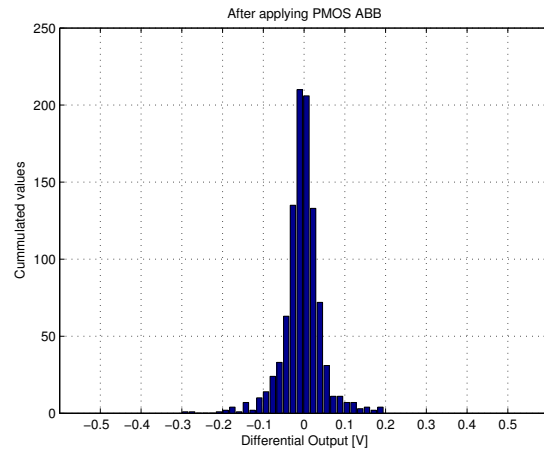


Figure 5. Histogram of the differential output with PMOS ABB correction.

the mismatches, while the differential stage was supplied with a common-mode input of $V_{dd}/2$. An illustrative plot of the measured output differential voltage without applying any correction is presented in Fig. 3, for 1000 Monte Carlo steps. When the stage is perfectly matched, the differential output should be on zero. The estimated standard deviation was 129.5 mV . Fig. 4 shows the simulation results after applying the PMOS ABB. After 1 ns , the *Calib_Start* control signal enables the body bias by switching the bulk contacts from V_{dd} to the output of the charge pumps. As a result, the variations-induced offset decreases, resulting in a substantially smaller offset dispersion, as shown in Fig. 4.

To obtain an exact evaluation of the mismatch reduction, we have run 1000 Monte Carlo iterations and we have estimated the standard deviation of the output offset, before and after applying the body bias correction. The histogram of the differential output obtained from the simulations is

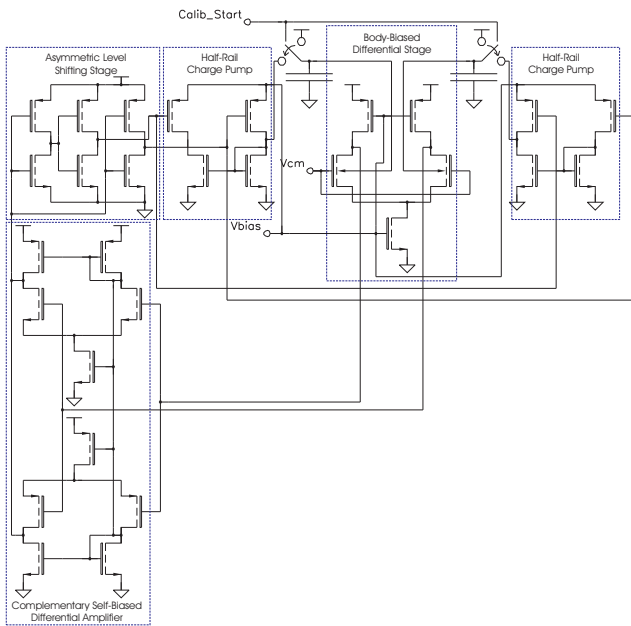


Figure 6. NMOS analog ABB circuit.

plotted in Fig. 5. We have obtained a significant improvement of the standard deviation with 63% (from 129.5 mV to 47.7 mV).

4.2. NMOS Analog ABB Circuit

The second implementation of our analog ABB method is depicted in Fig. 6. Here, we are connecting the ABB circuit to the bulk contacts of the NMOS pair. A few modifications of the circuit had to be made. First, the body bias range extends from ground to $V_{dd}/2$, therefore the charge pumps have been implemented with PMOS source-coupled differential stages. The half-rail swing is ensured with the same externally-fixed bias, as in the case of the PMOS ABB circuit, with the remark that here it serves as the upper limit of the body bias.

Since the charge pumps are now driven by PMOS transistors, the level shifting stage had to be redesigned accordingly. The non-inverting output switches now below $V_{dd}/2$, while the inverting branch switches above the half. This ensures that the outputs are both on V_{dd} when the transistor pairs are calibrated, such that the PMOS source-coupled pair of the charge pump is turned off.

Fig. 7 shows the results for 1000 iterations, where we obtained an improvement in standard deviation of 61% (from 140.2 mV to 54.1 mV). The correction capabilities are marginally lower than in the PMOS realization, with the same transistor count, but with the additional requirement of a triple-well process, which points out the advantage of applying the body bias on the PMOS load.

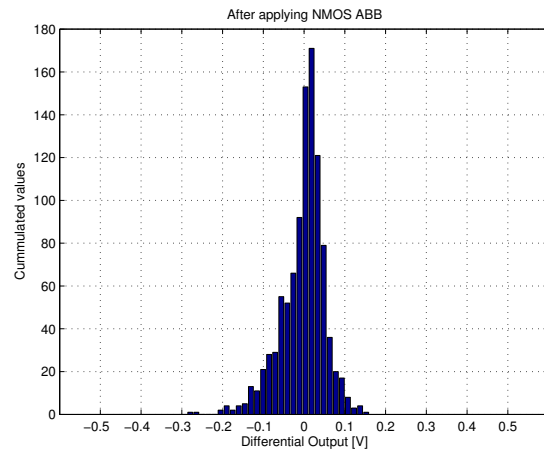


Figure 7. Histogram of the differential output with NMOS ABB correction.

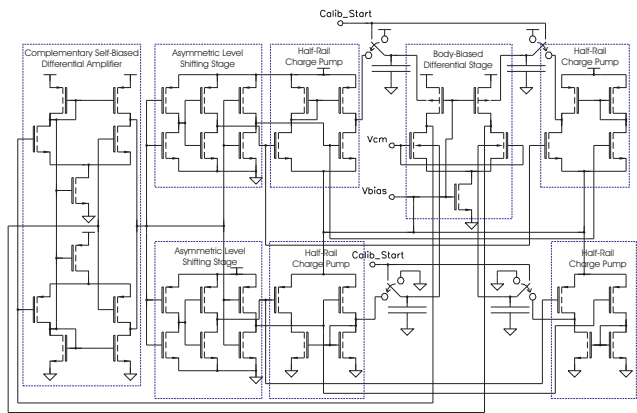


Figure 8. CMOS analog ABB circuit.

4.3. CMOS Analog ABB Circuit

In the most complex implementation of the analog ABB method, both the PMOS and the NMOS transistor pairs are calibrated through body biasing, as shown in Fig. 8. This implementation has the highest calibration potential, since it can adjust simultaneously all the four body biases to reduce the mismatch. One comparator, two level shifters (one for the PMOS and one for the NMOS pair), and four charge pumps (two for PMOS and two for NMOS calibration) are needed.

The results after 1000 Monte Carlo iterations are plotted in Fig. 9. The estimated standard deviation decreased with 73% (from 134 mV to 36 mV), proving that the CMOS ABB implementation achieves the best results amongst the three implementations, at the cost of a slight increase in transistor count and requiring a triple-well process.

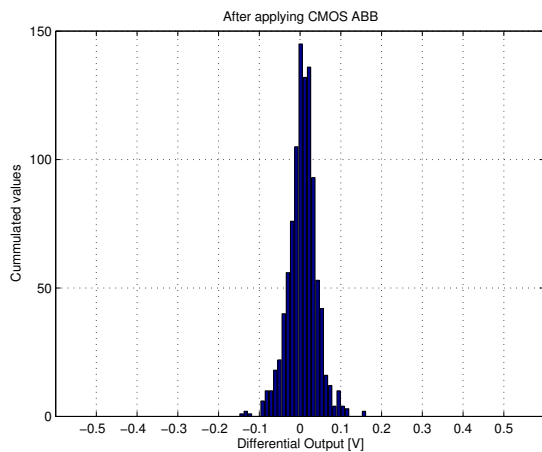


Figure 9. Histogram of the differential output with CMOS ABB correction.

5. Conclusions

In this paper, we presented a novel and efficient on-chip analog adaptive body bias method for reducing device mismatches in transistor pairs. The proposed method is highly appropriate for calibrations in analog and mixed-signal circuits, where perfectly-matched differential pairs and current mirrors are frequently required. We have implemented three circuit realizations with different transistor counts and correction capabilities. A PMOS, NMOS, and CMOS analog ABB implementation for a differential stage have been realized in a 90-nm, 1.0V technology from Infineon and achieved a 63%, 61%, and 73% reduction of the device mismatch in terms of standard deviation, respectively. The proposed method can be combined with classical techniques, such as device scaling, symmetric layout styles, and dummy insertions for achieving even better mismatch correction results.

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