

# technical programme topic chairs



**System Design Methods & Case Studies**  
**Harry Hsieh**  
 UC Riverside, US



**Analogue & Mixed AD Systems**  
**Angel Rodriguez-Vazquez**  
 CNM/IMSE, ES



**Design of Low-Power Systems & Case Studies**  
**Christian Piguet**  
 CSEM, CH



**Microarchitectural & Architectural Design**  
**Todd Austin**  
 The University of Michigan, US



**Reconfigurable Computing**  
**Walid Najjar**  
 UC Riverside, US



**Innovative & Emerging Technologies, Systems & Applications**  
**Vijaykrishnan Narayanan**  
 Pennsylvania State U, US



**Multi-Processors & Networks on Chip**  
**Luca Benini**  
 DEIS - Bologna U, IT



**System-Level Specification & Modelling**  
**Satnam Singh**  
 Microsoft, US



**Simulation & Emulation**  
**Mostapha Aboulhamid**  
 Montreal U, CA



**System Synthesis & Optimisation**  
**Juergen Teich**  
 Erlangen-Nuremberg U, DE



**Architectural Synthesis**  
**Roman Hermida**  
 UC Madrid, ES



**Logic & Technology Dependent Synthesis for Deep Submicron Circuits**  
**Tiziano Villa**  
 PARADES, IT



**Physical Design & Verification**  
**Andreas Kuehlmann**  
 Cadence, DE



**System Design Methods & Case Studies**  
**Grant Martin**  
 Tensilica, US



**Analogue & Mixed AD Systems**  
**Manfred Glesner**  
 TU Darmstadt, DE



**Design of Low-Power Systems & Case Studies**  
**Tajana Simunic**  
 UC San Diego, US



**Microarchitectural & Architectural Design**  
**Stamatis Vassiliadis**  
 TU Delft, NL



**Reconfigurable Computing**  
**Wayne Luk**  
 Imperial College London, UK



**Innovative & Emerging Technologies, Systems & Applications**  
**Christian Paulus**  
 Siemens, DE



**Multi-Processors & Networks on Chip**  
**Kees Goossens**  
 Philips, NL



**System-Level Specification & Modelling**  
**Ian Oliver**  
 Nokia, FI



**Simulation & Emulation**  
**Franco Fummi**  
 Verona U, IT



**System Synthesis & Optimisation**  
**Nikil Dutt**  
 UC Irvine, US



**Architectural Synthesis**  
**Fabrizio Ferrandi**  
 Politecnico di Milano, IT



**Logic & Technology Dependent Synthesis for Deep Submicron Circuits**  
**Jordi Cortadella**  
 UP Catalunya, ES



**Physical Design & Verification**  
**Juergen Koehl**  
 IBM, DE



**CAD for Analogue & Mixed-Signal Design, Symbolic Techniques**  
**Lars Hedrich**  
 Hannover U, DE



**Interconnect, EMC & Packaging Modelling**  
**Peter Feldmann**  
 IBM, US



**Formal Verification**  
**Rolf Drechsler**  
 Bremen U, DE



**Power Estimation & Optimisation**  
**Roberto Zafalon**  
 STMicroelectronics, IT



**Defect-Based Testing & Test of Regular Structures**  
**Jaume Segura**  
 Illes Balears U, ES



**Analogue, Mixed-Signal, RF & Mixed-Technology Test**  
**Adoracion Rueda**  
 IMSE/CNM, ES



**Test Generation, Simulation & Diagnosis**  
**Matteo Sonza Reorda**  
 Politecnico di Torino, IT



**BIST & Design for Testability**  
**Hans-Joachim Wunderlich**  
 Stuttgart U, DE



**SoC/SoB & Systems Test**  
**Rainer Dorsch**  
 IBM, DE



**On-Line Testing, Fault Tolerance & Reliability**  
**Cecilia Metra**  
 Bologna U, IT



**Real-Time Systems**  
**Gerhard Fohler**  
 Malardalens U, SE



**Compilers, Architectures & SW Synthesis for Embedded Systems**  
**Alex Dean**  
 North Carolina State U, US



**Embedded Software Technology**  
**Janos Sztipanovits**  
 Vanderbilt U, US



**CAD for Analogue & Mixed-Signal Design, Symbolic Techniques**  
**Gerd Vandersteen**  
 IMEC, BE



**Interconnect, EMC & Packaging Modelling**  
**Eric Beyne**  
 IMEC, BE



**Formal Verification**  
**Valeria Bertacco**  
 University of Michigan, US



**Power Estimation & Optimisation**  
**Eike Schmidt**  
 ChipVision Design, DE



**Defect-Based Testing & Test of Regular Structures**  
**Rob Aitken**  
 Artisan, US



**Analogue, Mixed-Signal, RF & Mixed-Technology Test**  
**Abhijit Chatterjee**  
 Georgia Tech., US



**Test Generation, Simulation & Diagnosis**  
**Patrick Girard**  
 LIRMM, FR



**BIST & Design for Testability**  
**Sybille Hellebrand**  
 Paderborn U, DE



**SoC/SoB & Systems Test**  
**Erik Jan Marinissen**  
 Philips, NL



**On-Line Testing, Fault Tolerance & Reliability**  
**Fabrizio Lombardi**  
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**Real-Time Systems**  
**Sanjoy Baruah**  
 North Carolina U, US



**Compilers, Architectures & SW Synthesis for Embedded Systems**  
**Hans van Someren**  
 ACE Associated Compiler Experts, NL



**Embedded Software Technology**  
**Manfred Broy**  
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