

Tutorial And Panel Session
Low-Power Design Tools: Are EDA Vendors Taking this Matter Seriously?

Organizers: E Macii, Politecnico di Torino, IT
M Casale-Rossi, Synopsys Inc, IT

Panel Moderator: G De Micheli, EPFL Lausanne, CH

Tutorial Speakers: E Macii, Politecnico di Torino, IT
M Pedram, Southern California U, US

Panelists: D Friebel, Nokia, DE
R Aitken, ARM, US
A Domic, Synopsys, US
R Zafalon, STMicroelectronics, IT

Abstract: While transistors per square millimeter and on-chip clock keep scaling smoothly according to Moore's Law, V_{dd} does not, nor does V_{th} . This leads to a dramatic increase in chip power density, and to a significant shift in the balance between dynamic and leakage power. In spite of the recent effort made by EDA vendors in delivering novel solutions that help mitigating the effects on power consumption of technology scaling, the question of whether EDA industry is taking the low-power matter seriously still remains.

This session will provide an answer to this intriguing question, by first offering a short review of the state-of-the-art in design technologies for dynamic and leakage power minimisation. The session will then continue with a public "trial", in which OEMs, IDMs, IP and fabless semiconductor vendors will play the role of the public prosecutor, against defendant EDA industry. The court's ruling will tell us about the future targets the EDA vendors will pursue in low-power design technologies.