

Tutorials

A1: System Modelling with SystemC

Organizer: Rachael Mahoney, Doulos, UK

Speaker: John Aynsley, Doulos, UK

Complexities of present systems or SoC designs are forcing the movement to a higher level of abstraction than RTL. With most of the system containing a large portion of software, the present languages, methodologies and tools are not adequate to tackle system-level design. SystemC is a C++ class library aimed at modelling systems with hardware and software content at many different levels of abstraction and using mixed models of computation. SystemC is already being proven in an industrial context for the transaction-level modelling of bus and processor based systems, where it excels.

This tutorial includes an overview of SystemC, an introduction to the key features of SystemC version 2.0, a discussion of the main abstraction levels, and a case study showing the practical use of SystemC for transaction-level modelling. A case study example design is refined from an abstract untimed functional (UTF) model using abstract fifo channels through a timed functional (TF) model to a transaction-level bus model, and finally to a cycle-accurate (CA) model including both hardware and software elements. A simple example of hardware-software partitioning is shown. The SystemC refinement process is discussed, including the use of SystemC interfaces during communication refinement. The issues of performance and accuracy of the SystemC simulation are considered in the context of the various abstraction levels.

B1: Recent Advances in Verification, Equivalence Checking and SAT-Solvers

Organizer: Dhiraj Pradhan, Bristol U, UK

Speakers: Dhiraj Pradhan, Bristol U, UK; Magdy Abadir, Motorola, US; Li-C Wang, UC Santa Barbara, US

This tutorial provides an overview of recent developments as well as basic principles in verification, equivalence checking and SAT-Solvers. It also provides a perspective of practical industrial experiences in the use and development of the tools.

In the first part the design flow and the role of RTL verification will be described. An overview of techniques will be given, including simulation-based techniques, basic concepts of equivalence checking, combinational equivalence checking, ATPG-based techniques. Also an overview of solvers will be given (structural verification, BDD-based solvers, SAT-based solvers). The role of Decision Diagrams (BDDs, zBDDs, mBDDs) will be discussed. In the second part concepts of SAT solvers are discussed, and some new EDA-related techniques are presented. Finally, the tutorial will give an overview of various commercially available tools and their applicability. Also future challenges will be lined out, such as design for verifiability, and potential new directions will be given.

C1: Mixed-Signal Design Using Verilog-AMS and VHDL-AMS

Organizer: Olaf Zinke, Cadence, US

Speaker: Olaf Zinke, Cadence, US

With the evolution towards highly integrated systems (SoC's) in ultra deep submicron CMOS technologies, more and more of these systems become mixed-signal, containing also analogue and/or RF parts. The design complexity for these mixed-signal systems requires new design methodologies.

This tutorial will give an introduction to language-based mixed-signal design methodologies. The tutorial will point out how the different analogue and digital design styles converge in the design environment. The use of Verilog-AMS as a design language and VHDL-AMS as a modelling language will be demonstrated. Examples are given on how the mixed-signal capabilities of these languages can be used to reduce the simulation time of mixed-signal systems.

D1: Infrastructure IP for SoC Yield

Organizer: Dimitris Gizopoulos, Piraeus U, GR
Speaker: Yervant Zorian, Virage Logic, US

In addition to the functional IP cores, today's Systems on Chip (SoC's) necessitate embedding a special family of IP blocks, called Infrastructure IP blocks. These are meant to ensure the manufacturability of the SoC and to achieve adequate levels of yield and reliability. The Infrastructure IP leverages the manufacturing knowledge and feeds back the information into the design phase.

This tutorial analyses the key trends and challenges resulting in manufacturing susceptibility and field reliability that necessitates the use of such Infrastructure IP. Then it concentrates on several examples of such embedded IP's for detection, analysis and correction.

This Tutorial is part of the IEEE Computer Society TTTC Test Technology Educational Program (TTEP) 2003.

A2: Reconfigurable Computing: Fundamentals, Architectures and Tools

Organizer: Andreas Koch, TU Braunschweig, DE
Speaker: Andreas Koch, TU Braunschweig, DE

Reconfigurable computing is an important architectural approach in a time of growing chip capacities and increasing demands on flexibility. This tutorial aims to introduce professionals experienced with conventional chip and system design methods to the concept of Reconfigurable Computing. The audience should be familiar with HDLs such as Verilog and have at least a passing acquaintance with programming in a software language such as C. The lecture will discuss tool flows and show examples of inputs and outputs.

In the first part of the tutorial fundamentals of reconfigurable computing will be discussed and its use will be motivated by some successful examples. The second part will examine different architectural choices for integrating reconfigurable components into a large hardware system, and will present a practical example of a reconfigurable co-processor. The third part discusses design flows for reconfigurable systems. This will cover both manual HDL-based programming as well as programming by automatic compilation from a high-level language. It will also be discussed how to exploit the reconfigurability aspect of such a system. Finally, some practical considerations will be given with an overview of commercial reconfigurable off-the-shelf devices, reconfigurable IP blocks and software tools.

B2: Performance Analysis in Communication-Centric SoC Design

Organizer: Rolf Ernst, TU Braunschweig, DE
Speakers: Rolf Ernst, TU Braunschweig, DE; Andreas Herkersdorf, IBM, CH; Lothar Thiele, ETH Zurich, CH

Performance simulation is current industrial practice in complex system design. As is well known, there are serious limitations concerning run-time and simulation coverage. On the other hand, there has been major progress in analytical methods that may complement or even replace performance simulation. This tutorial presents these new analytical methods and demonstrates them on a practical design case.

The first part of the tutorial will give an overview on the problem of performance modeling and estimation, starting from a single process to complex communication-centric heterogeneous systems. The second talk will introduce an important application domain of network processors in which performance evaluation is of highest importance for design optimisation and verification analysis has proven itself. The third talk will demonstrate how to apply formal analysis to network processor design.

C2: Modelling and Simulation Methods for High-Frequency Systems

Organizer: Georges Gielen, KU Leuven, BE

Speakers: Joel Phillips, Cadence, US; Luis Miguel Silveira, TU Lisbon, PT

The frequencies in many electronic systems keep on increasing. This involves both the clock speeds in digital systems, as well as the operating frequencies in RF circuits.

This tutorial is concerned with physical modelling and verification of high-frequency systems. Topics to be covered include parasitic and substrate modelling as well as modelling of sub-systems including frequency-described modules. The presenters will also discuss various issues in simulation, including model order reduction and algorithms for analysis and verification of RF circuits.

D2: Failure Modes in Nanometer Technologies

Organizer: Dimitris Gizopoulos, Piraeus U, GR

Speakers: Chuck Hawkins, New Mexico U, US; Jaume Segura, Balearic Islands U, ES

Process technology scaling has brought current manufacturing processes to the 100 nm region and below. The behavior of IC devices and the interconnect system in nanometer technologies brings new physical effects that, in addition to traditional well-known failure modes, open new challenges in IC testing. In this tutorial we will describe the electronic and physical basis to understand the varieties of CMOS failure mechanisms in up-to-date scaled technologies.

The tutorial will start with an overview of the traditional defect models and test solutions, leading to an analysis of the failure mechanisms in nanometer technologies. Finally, the appropriate test strategies will be presented.

This Tutorial is part of the IEEE Computer Society TTTC Test Technology Educational Program (TTEP) 2003.