

Technical Program Chairs



SYSTEM DESIGN METHODS
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Politecnico di Torino, IT



SYSTEM DESIGN METHODS
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ANALOGUE & MIXED A/D SYSTEMS
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IMEC, BE



ANALOGUE & MIXED A/D SYSTEMS
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DESIGN OF LOW POWER SYSTEMS
Wolfgang Nebel
Oldenburg U & OFFIS, DE



DESIGN OF LOW POWER SYSTEMS
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Southern California U, US



PLATFORM DESIGN
Ralf Seepold
Carlos III de Madrid U, ES



PLATFORM DESIGN
Teresa Riesgo
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RECONFIGURABLE COMPUTING
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FZI/Tuebingen U, DE



RECONFIGURABLE COMPUTING
Kurt Keutzer
UC Berkeley, US



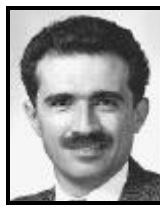
SYNCHRONIZATION METHODS
Marc Renaudin
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SYNCHRONIZATION METHODS
Rajit Manohar
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MULTIPROCESSOR & NETWORKS ON CHIP
Ahmed Jerraya
TIMA, Grenoble, FR



MULTIPROCESSOR & NETWORKS ON CHIP
Giovanni De Micheli
Stanford U, US



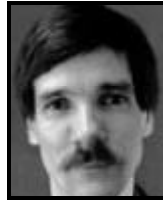
SYSTEM LEVEL
SPECIFICATION
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SYSTEM LEVEL
SPECIFICATION
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Royal Inst. of Technology, SE



REAL-TIME EMBEDDED
SYSTEMS
Zebo Peng
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REAL-TIME EMBEDDED
SYSTEMS
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SIMULATION &
EMULATION
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HW/SW CODESIGN
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ARCHITECTURAL
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LOGIC & FSM SYNTHESIS
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PHYSICAL DESIGN &
VERIFICATION
Ralph Otten
TU Eindhoven, NL



PHYSICAL DESIGN &
VERIFICATION
Frank Johannes
TU Munich, DE



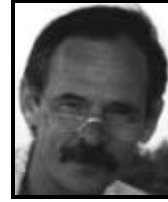
CAD FOR ANALOG
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TU Munich, DE



CAD FOR ANALOG
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Alcatel R&I, FR



INTERCONNECT, EMC &
PACKAGING
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INTERCONNECT, EMC &
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FORMAL VERIFICATION
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COLLABORATIVE
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POWER ESTIMATION &
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DEFECT BASED TESTING
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ANALOG & MIXED SIGNAL
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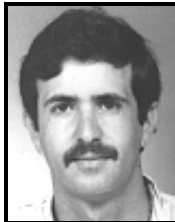
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TEST PARTITIONING & SoC
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TEST PARTITIONING &
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